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Analog-to-Digital Conversion Architectures

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5.1 Introduction

Digital signal processing methods fundamentally require that signals are quantized at discrete time instances and represented as a sequence of words consisting of 1's and 0's. In nature, signals are usually nonquantized and continuously varied with time. Natural signals such as air pressure waves as a result of speech are converted by a transducer to a proportional analog electrical signal. Consequently, it is necessary to perform a conversion of the analog electrical signal to a digital representation or vice versa if an analog output is desired. The number of quantization levels used to represent the analog signal and the rate at which it is sampled is a function of the desired accuracy, bandwidth that is required, and the cost of the system. Figure 5.1 shows the basic elements of a digital signal processing system. The analog signal is first converted to a discrete time signal by a sample and hold circuit. The

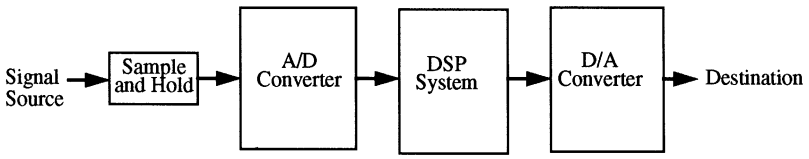

FIGURE 5.1: Digital signal processing system.

output of the sample and hold is then applied to an analog-to-digital converter (A/D) circuit where the sampled analog signal is converted to a digitally coded signal. The digital signal is then applied to

the digital signal processing (DSP) system where the desired DSP algorithm is performed. Depending on the application, the output of the DSP system can be used directly in digital form or converted back to an analog signal by a digital-to-analog converter (D/A). A digital filtering application may produce an analog signal as its output, whereas a speech recognition system may pass the digital output of the DSP system to a computer system for further processing. This section will describe basic converter terminology and a sample of common architectures for both conventional Nyquist rate converters and oversampled delta-sigma converters.

5.2 Fundamentals of A/D and D/A Conversion

The analog signal can be given as either a voltage signal or current signal, depending on the signal source. Figure 5.2 shows the ideal transfer characteristics for a 3-bit A/D conversion. The output of

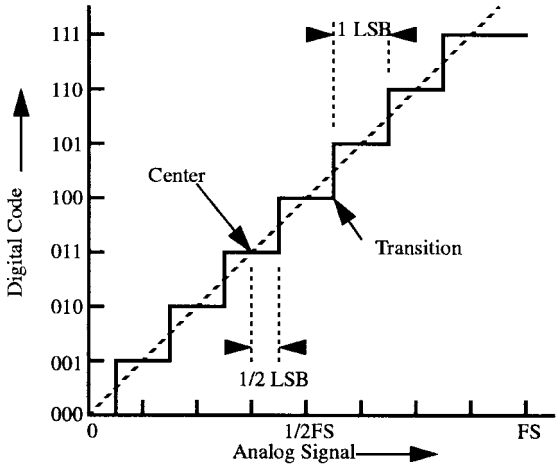

FIGURE 5.2: Ideal transfer characteristics for an A/D converter.

the converter is an n-bit digital code given as,

$$D = \frac{A_{sig}}{FS} = \frac{b_n}{2^n} + \frac{b_{n-1}}{2^{n-1}} + \ldots + \frac{b_1}{2^1} \tag{5.1}$$

where A_{sig} is the analog signal, FS is the analog full scale level, and b_n is a digital value of either 0 or 1. As shown in the figure, each digital code represents a quantized analog level. The width of the quantized region is one least-significant bit (LSB) and the ideal response line passes through the center of each quantized region. The converse D/A operation can be represented as viewing the digital code in Fig. 5.2 as the input and the analog signal as the output. An n-bit D/A converter transfer equation is given as

$$A_{sig} = FS\left(\frac{b_n}{2^n} + \frac{b_{n-1}}{2^{n-1}} + \ldots + \frac{b_1}{2^1}\right) \tag{5.2}$$

where A_{sig} is the analog output signal, FS is the analog full scale level and b_n is a binary coefficient.

The *resolution* of a converter is defined as the smallest distinct change that can be resolved (pro-

duced) at an analog input (output) for an A/D (D/A) converter. This can be expressed as

$$\Delta A_{sig} = \frac{FS}{2^N} \tag{5.3}$$

where ΔA_{sig} is the smallest reproducible analog signal for an N-bit converter with full scale analog signal of FS.

The *accuracy* of a converter, often referred to also as *relative accuracy*, is the worst-case error between the actual and the ideal converter output after gain and offset errors are removed [1]. This can be quantified as the number of equivalent bits of resolution or as a fraction of an LSB.

The *conversion rate* specifies the rate at which a digital code (analog signal) can be accurately converted into an analog signal (digital code). Accuracy is often expressed as a function of conversion rate and the two are closely linked. The conversion rate is often an underlying factor in choosing the converter architecture. The speed and accuracy of analog components are a limiting factor. Sensitive analog operations can either be done in parallel, at the expense of accuracy, or cyclicly reused to allow high accuracy with lower conversion speeds.

5.2.1 Nonideal A/D and D/A Converters

Actual A/D and D/A converters exhibit deviations from the ideal characteristics shown in Fig. 5.2. Integration of a complete converter on a single monolithic circuit or as a macro within a very large scale integration (VLSI) DSP system presents formidable design challenges. Converter architectures and design trade-offs are most often dictated by the fabrication process and available device types. Device parameters such as voltage threshold, physical dimensions, etc. vary across a semiconductor die. These variations can manifest themselves into errors. The following terms are used to describe converter nonideal behavior:

1. *Offset error*, described in Fig. 5.3, is a d.c. error between the actual response with the ideal response. This can usually be removed by trimming techniques.

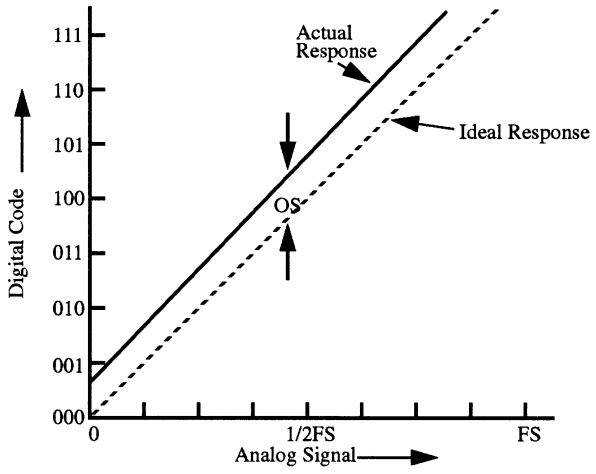

FIGURE 5.3: Offset error.

2. *Gain error* is defined as an error in the slope of the transfer characteristic shown in Fig. 5.4, which can also usually be removed by trimming techniques.

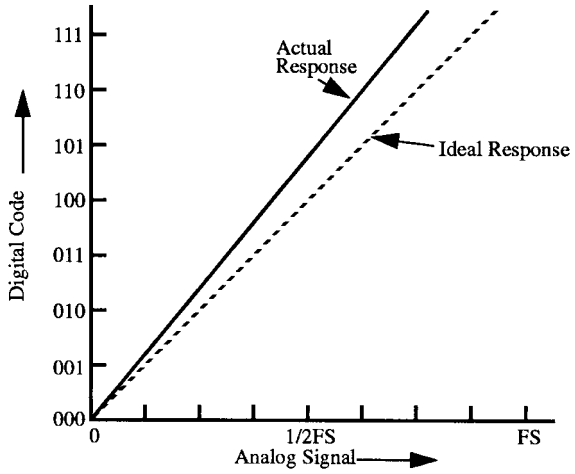

FIGURE 5.4: Gain error.

3. *Integral nonlinearity* is the measure of worst-case deviation from an ideal line drawn between the full scale analog signal and zero. This is shown in Fig. 5.5 as a monotonic nonlinearity.

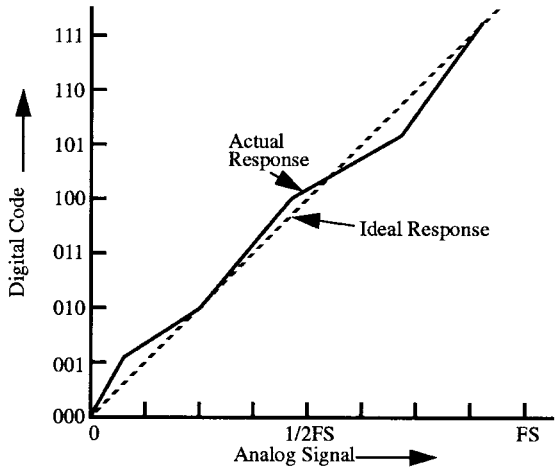

FIGURE 5.5: Monotonic nonlinearity.

4. *Differential nonlinearity* is the measure of nonuniform step sizes between adjacent steps in a converter. This is usually specified as a fraction of an LSB.
5. *Monotonicity* in a converter specifies that the output will increase with an increasing input. Certain converter architectures can guarantee monotonicity for a specified number of bits of resolution. A nonmonotonic transfer characteristic is detailed in Fig. 5.6.
6. *Settling time* for D/A converters refers to the time taken from a change of the digital code to the point at which the analog output settles within some tolerance around the final value.

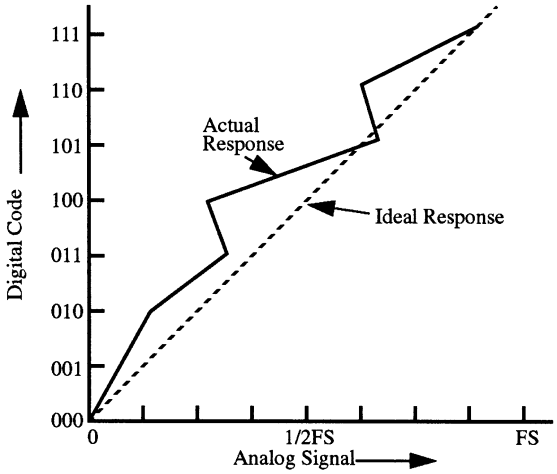

FIGURE 5.6: Nonmonotonic nonlinearity.

7. *Glitches* can occur during changes in the output at major transitions, i.e., at 1 MSB, 1/2 MSB, 1/4 MSB. During large changes, switching time delays between internal signal paths can cause a spike in the output.

The choice of converter architecture can greatly affect the relative weight of each of these errors. Data converters are often designed for low cost implementation in standard digital processes, i.e., digital CMOS, which often do not have well-controlled resistors or capacitors. Absolute values of these devices can vary by as much as $\pm$ 20% under typical process tolerances. Post-fabrication trimming techniques can be used to compensate for process variations, but at the expense of added cost and complexity to the manufacturing process. As will be shown, various architectural techniques can be used to allow high speed or highly accurate data conversion with such variations of process parameters.

5.3 Digital-to-Analog Converter Architecture

The digital-to-analog (D/A) converter, also known as a DAC, decodes a digital word into a discrete analog level. Depending on the application, this can be either a voltage or current. Figure 5.7 shows a high level block diagram of a D/A converter. A binary word is latched and decoded and drives a set of switches that control a scaling network. A basic analog scaling network can be based on voltage scaling, current scaling, or charge scaling [1, 2]. The scaling network scales the appropriate analog level from the analog reference circuit and applies it to the output driver. A simple serial string of identical resistors between a reference voltage and ground can be used as a voltage scaling network. Switches can be used to tap voltages off the resistors and apply them to the output driver. Current scaling approaches are based on switched scaled current sources. Charge scaling is achieved by applying a reference voltage to a capacitor divider using scaled capacitors where the total capacitance value is determined by the digital code [1]. Choice of the architecture depends on the available components in the target technology, conversion rate, and resolution. Detailed description of these trade-offs and designs can be found in the references [1]–[5].

5.4 Analog-to-Digital Converter Architectures

The analog-to-digital (A/D) converter, also known as an ADC, encodes an analog signal into a digital word. Conventional converters work by sampling the time varying analog signal at a sufficient rate to fully resolve the highest frequency components. According to the sampling theorem, the minimum sampling rate is twice the frequency of the highest frequency contained in the signal source. The sampling rate requirement thus becomes the major deterministic factor in choosing a proper converter architecture. Certain architectures exploit parallelism to achieve high speed operation on the order of 100's of MHz, and others which can be used for high accuracy 16-bit resolution for signals with maximum frequencies on the order of 10's of KHz.

5.4.1 Flash A/D

The flash A/D, also known as a parallel A/D, is the highest speed architecture for A/D conversion since maximum parallelism is used. Figure 5.8 shows a block diagram of a 3-bit flash A/D converter. A flash converter requires $2^n - 1$ analog comparators, $2^n - 1$ reference voltages, and a digital encoder. The reference voltages are required to be evenly spaced between 0.5 LSB above the most negative signal and 1.5 LSB below the most positive signal and spaced 1 LSB apart. Each reference voltage is applied to the negative input of a comparator and the analog signal voltage is applied simultaneously to all the comparators. A thermometer code results at the output of the comparators which is converted to a digital word by encoding logic. The speed of the converter is limited by the time delay through a comparator and the encoding logic. This speed is gained at the expense of accuracy, which is limited by the ability to generate evenly spaced reference voltages and the precision of the comparators. Each analog comparator must be precisely matched in order to achieve acceptable performance at a given resolution. For these reasons, flash A/D converters are typically used only for very high speed low resolution applications.

5.4.2 Successive Approximation A/D Converter

A successive approximation A/D converter is formed creating a feedback loop around a D/A converter. Figure 5.9 shows a block diagram for an 8-bit successive approximation A/D. The operation of the converter works by initializing the successive approximation register (SAR) to a value where all bits are set to 0 except the MSB which is set to 1. This represents the mid-level value. The analog signal is applied to a sample-and-hold (S/H) circuit, and on the first clock cycle the DAC converts the digital code stored in the SAR into an analog signal. The comparator is used to determine whether the analog signal is greater or less than the mid level, and control logic determines whether to leave the MSB set to 1 or to change it back to 0. The process is repeated on the next clock cycle, but instead the next MSB is tested. For an n-bit converter n clock cycles are required to fully quantize each sample-and-hold signal. The speed of the successive approximation converter is largely limited by the speed of the DAC and the time delay through the comparator. This type of converter is widely used for medium speed and medium accuracy applications. The resolution is limited by the DAC converter and the comparator.

5.4.3 Pipelined A/D Converter

A pipelined A/D converter achieves high-speed conversion and high accuracy at the expense of latency in the conversion process. A pipelined A/D converter block diagram is shown in Fig. 5.10. The conversion process is broken into multiple stages where, at each stage, a partial conversion is done and the converted bits are shifted down the pipeline in digital registers. Figure 5.11 shows the detail of a single pipeline stage. The analog signal is applied to a sample-and-hold circuit and

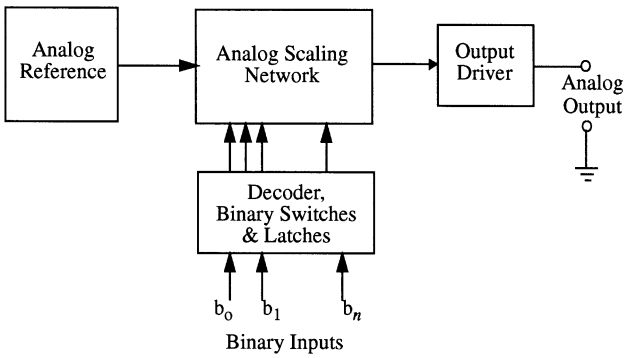

FIGURE 5.7: Basic D/A converter block diagram.

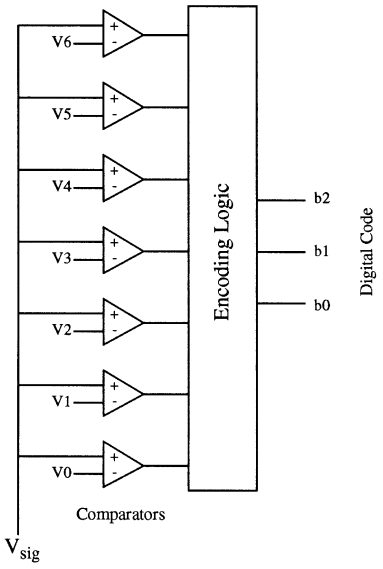

FIGURE 5.8: 3-bit flash A/D converter.

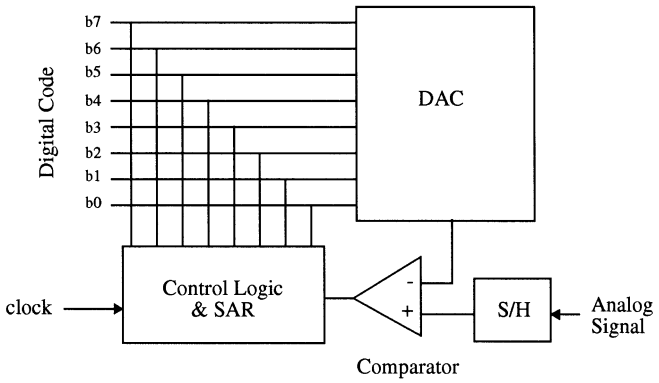

FIGURE 5.9: 8-bit successive approximation A/D converter.

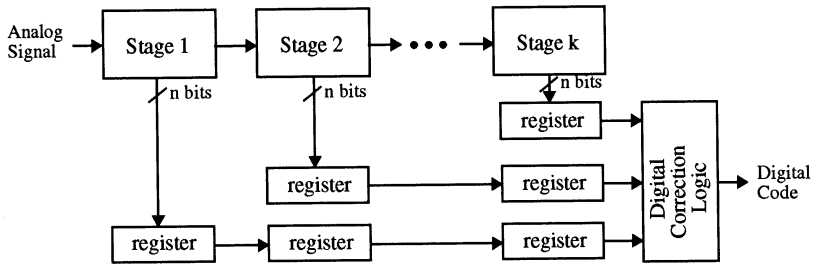

FIGURE 5.10: Pipelined A/D converter.

the output is applied to an n-bit flash ADC where n is less then the total desired resolution. The outputs of the ADC are connected directly to a DAC, and the output of the DAC is subtracted from the original analog signal stored in the S/H to produce a residual signal. The residual signal is then amplified by 2^n so that it will vary within the entire full scale range of the next stage and is transferred on the next clock cycle. At this point the first stage begins conversion on the next analog sample. The maximum conversion rate is determined by the time delay through a single stage. Pipelining allows high resolution conversion without the need for many comparators. An 8-bit converter can be ideally constructed with $k = 4$ stages with $n = 2$ bits of resolution per stage, requiring only 12 total comparators. This can be contrasted with an 8-bit flash converter requiring 255 comparators. Each pipeline stage adds an additional cycle of latency before the final code is converted. Pipelined converters also accommodate digital correction schemes for errors generated in the analog circuitry. Digital correction can be achieved by using higher resolution ADC and DAC circuits in each stage than required so that errors in the preceding stage can be detected and corrected digitally [5]. Auto calibration can also be achieved by adding additional stages after the required stages to convert errors in the DAC values and storing these digitally to be added to the final result [6].

5.4.4 Cyclic A/D Converter

Cyclic A/D converters, also known as algorithmic converters, trade off conversion speed for high accuracy without the need for calibration or device trimming. Figure 5.12 shows a block diagram of a cyclic A/D converter [5]. Here the same analog components are cyclicly reused for conversion of each bit for each analog sample. The conversion process works by initially sampling the input signal by setting switch S1 appropriately. The sampled signal is then amplified by a factor of two and applied

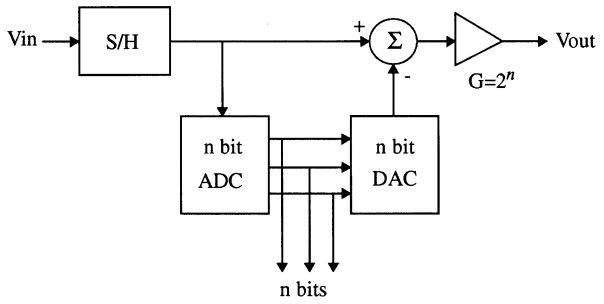

FIGURE 5.11: Diagram of single pipelined A/D converter stage.

to a comparator where it is compared to a reference level, Vref. If the voltage exceeds the reference level, a bit value of 1 is produced and the reference voltage is subtracted from the amplified signal by control of switch S2 to produce the residual voltage V_e. If the amplified signal is less than the reference voltage, Vref, the comparator outputs a 0, and V_e represents the unchanged amplified signal. On the remaining cycles for the sample, switch S1 changes so that the residual voltage V_e is applied to the S/H circuit. The cycle is repeated for each remaining bit. Operation on the conversion process produces a serial stream of digital bit values from output of the comparator. An n-bit converter requires n conversion cycles for each sampled signal.

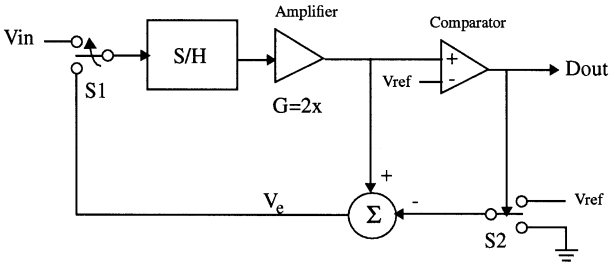

FIGURE 5.12: Block diagram of a cyclic A/D converter.

5.5 Delta-Sigma Oversampling Converter

The oversampling delta-sigma A/D converter was first proposed 30 years ago [7], while it only became popular after the maturity of the VLSI digital technology. With the advancement of semiconductor technology, an increasing portion of signal processing tasks have been shifted from the usual analog domain to digital domain. For digital systems to interact with analog signal sources, such as voice, data, and video, the role of analog-to-digital interface is essential. In voice data processing and communication, an accurate digital form is often desired to represent the voice. Due to the large demand of these systems, the cost must be kept at a minimum. All these requirements call upon a need to implement monolithic high resolution analog-to-digital interfaces in economical semiconductor technology. However, with the increasing complexity of integration and a trend of reducing supply voltage, the accuracy of device components and analog signal dynamic range

deteriorate. It becomes more difficult to realize high resolution conversions by conventional Nyquist rate converter architecture.

Compared to Nyquist rate converters, the oversampling converters use coarse analog components at the front end and employ more digital signal processing in the later stages. High resolution conversions are achieved by trading off speed and digital signal processing complexity, both of which can be easily realized in modern VLSI technology.

The oversampling A/D converter and Nyquist rate converter are compared in Fig. 5.13. A nonoversampled A/D converter has an anti-aliasing lowpass filter in the front. The anti-aliasing filter attenuates high-frequency components buried in the analog input and prevents them from being aliased into the signal frequency band. Because the converter is sampled at the Nyquist rate, which is twice the input signal bandwidth, the anti-aliasing filter's transition band must be very narrow and its stop-band must have enough suppression of the out-of-band noise. This requirement makes the filter very complex and adds to the complexity that a nonoversampled A/D already has.

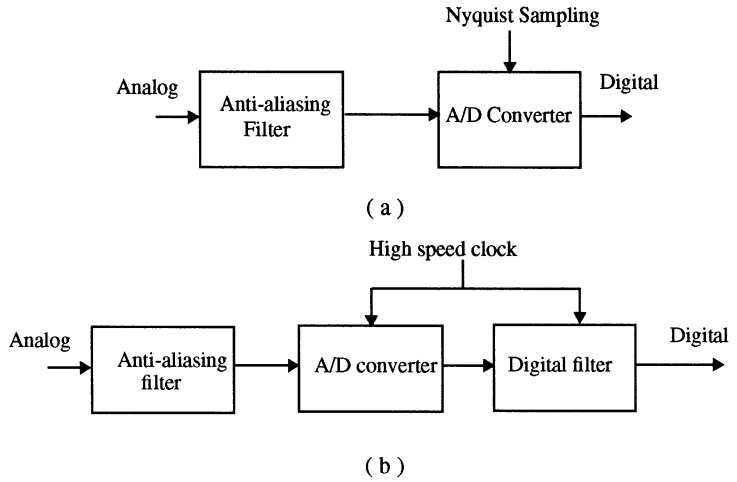

FIGURE 5.13: (a) Nonoversampled A/D converter. (b) oversampled A/D converter.

In comparison, an oversampled delta-sigma A/D converter, as shown in Fig. 5.13(b), is sampled at a higher rate than the input Nyquist rate. A simple first-order lowpass filter is sufficient to attenuate the noise components at the sampling frequency region to avoid the noise aliasing. This is because only the noise components close to the sampling frequency can be aliased back into the signal band. This arrangement simplifies the design and implementation of the filter. The complexity of the A/D itself is much simpler than the nonoversampled A/D converters as we will see later. The only extra complexity in the oversampled A/D converters is that more digital signal processing is required after the A/D conversion. But this becomes less and less an issue with the advancement of the VLSI technology. In the following sections, we will explain the conversion principle and various architectures of the oversampling delta-sigma converter.

5.5.1 Delta-Sigma A/D Converter Architecture

Delta-Sigma Oversampling A/D Converter Principle

The structure of a first-order delta-sigma converter is shown in Fig. 5.14. The input signal is

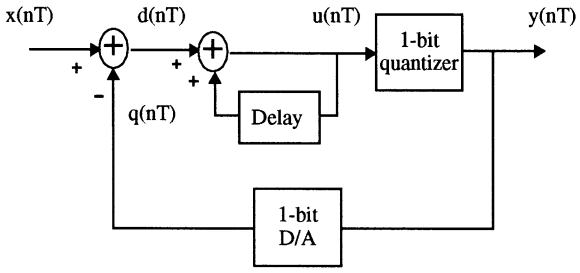

FIGURE 5.14: The modulator of a first-order delta-sigma converter. T is the sampling period and n is the index.

sampled at a frequency $f_s (T = 1/f_s)$. A feedback signal from a 1-bit D/A converter is subtracted from the input and the residue signal is accumulated by an integrator. The output of the integrator is quantized to generate a 1-bit digital stream. This digital output sets the sign of the feedback. If the digital output is **1**, it feeds back a large negative signal to subtract from the input signal. The net effect of the feedback loop is to keep the output of the integrator small so that the output digits always track the amplitudes of the input signal.

The resolution of an A/D converter is determined by the quantization noise generated in the process. Even though a delta-sigma converter only has an 1-bit quantizer, much higher resolution is achieved by employing the noise shaping mechanism to move the noise out of the signal band and later blocking it using a lowpass digital filter.

Quantization is a nonlinear process and the feedback mechanism makes the noise highly dependent on the input signal spectrum. Rigorous treatment of this noise component in a delta-sigma converter can be found in the literature [8]. Useful information can still be obtained by linearizing the quantization process. The noise component is approximated by white additive noise uniformly distributed up to half of the sampling frequency. This approximation is valid because over a long period of time, the input to the quantizer will spread over a large number of values and appear to be quasi-random, so the noise introduced is quasi-random as well. Similar to a nonoversampled A/D converter, the rms value of the noise is $e_{rms}^2 = \frac{\Delta^2}{12}$, where Δ is the quantization step. When the quantizer is sampled at f_s, the noise power is sampled into a frequency band: $0 \leq f < f_s/2$ and its spectral density is

$$Q(f) = \sqrt{2} \cdot e_{rms} \tag{5.4}$$

where f is normalized to f_{-s}.

The delta-sigma converter can be generalized as shown in Fig. 5.15. The forward path is modeled

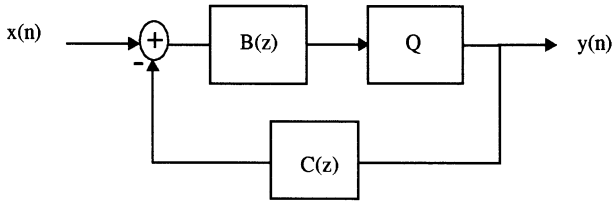

FIGURE 5.15: General feedback system.

by transfer function $B(z)$ plus the noise, and the feedback path can be modeled by $C(z)$. The system

output and input transfer function is governed by

$$Y(z) = \frac{B(z) \cdot X(z) + Q}{1 + B(z) \cdot C(z)} \tag{5.5}$$

To achieve high-resolution A/D conversion, the system needs to convert the input signal within a specified frequency bandwidth and minimize the noise component in that band. One method is to pass the signal component and block the noise component. This can be expressed as

$$Y(z) = X(z) + H_{ns}(z) \cdot Q \,, \tag{5.6}$$

where the input $X(z)$ passes through the system, but the quantization noise is modified by a noise-shaping function $H_{ns}(z)$.

Comparing Eq. 5.5 to Eq. 5.6, to achieve the noise-shaping effect, the system in Fig. 5.15 needs to have the following property:

$$\begin{aligned} C(z) &= 1 - \frac{1}{B(z)} \\ B(z) &= \frac{1}{H_{ns}(z)} \end{aligned} \tag{5.7}$$

Now, we can see the delta-sigma A/D converter shown in Fig. 5.14 as a noise-shaping data converter. The transfer function of the integrator in the forward pass is $\frac{1}{1-z^{-1}}$; the D/A converter in the feedback path is equivalent to a delay element and its transfer function is z^{-1}. They satisfy the relation required by a noise-shaping converter in Eq. 5.7. Therefore, its noise-shaping function $H_{ns}(z)$ is

$$H_{ns}(z) = \frac{1}{B(z)} = 1 - z^{-1} \tag{5.8}$$

which is a highpass filtering function. The amplitude of its response is

$$|H_{ns}(z)| = |1 - z^{-1}| = 2\sin(\pi f) \tag{5.9}$$

where f is the normalized frequency with respect to f_s. This function is plotted in Fig. 5.16. As shown in the figure, the noise is evenly distributed across the frequency, before applying the noise shaping function. The noise power in the signal band is the area of a region highlighted by the grey color underneath the flat line. After applying the noise-shaping function, the noise in the signal band is suppressed to a much lower level and the total noise power left (dark grey region) is much smaller than the original noise power. The high-frequency noise portion will be filtered by the digital filter. Therefore, the signal-to-noise ratio of the converter is greatly enhanced.

Quantitatively, the noise power left in the signal band is the integration of its spectrum up to signal bandwidth f_b as

$$N^2 = \int_0^{f_b/f_s} \left(|H_{ns}(z)|^2 Q^2 \right) df = \frac{2\Delta^2}{3f_s} \int_0^{f_b/f_s} [\sin(\pi f)]^2 \, df \tag{5.10}$$

where Q^2 is substituted for the noise spectral density in Eq. 5.4. In a delta-sigma converter the signal bandwidth is significantly lower than the sampling frequency. The resulting integration is

$$N_q^2 = \frac{2\pi^2\Delta^2}{9} \left(\frac{f_b}{f_s} \right)^3 \,. \tag{5.11}$$

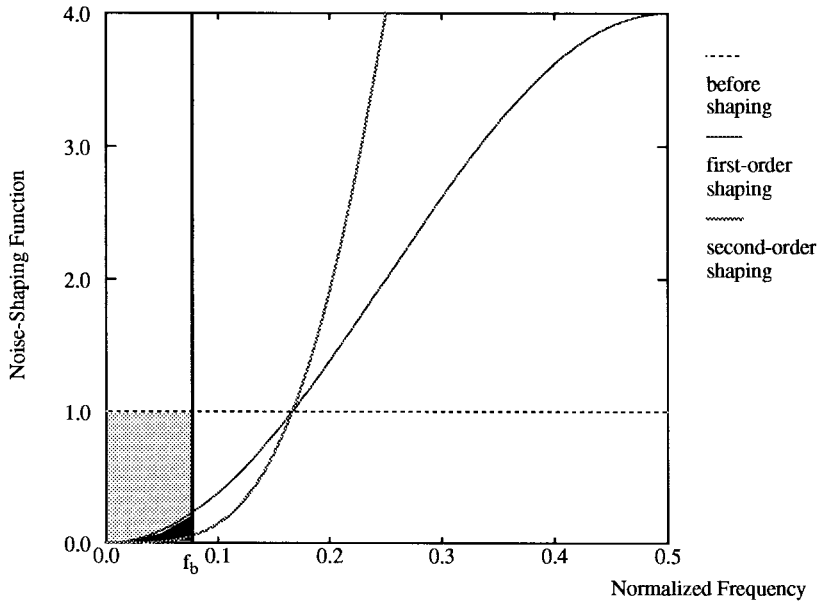

FIGURE 5.16: Plot of noise-shaping effect of the delta-sigma modulator comparing the noise power left within the baseband f_h. The noise (cross-hatched region) of a first-order modulator is much less than the noise before shaping (shaded region). Noise from the second-order shaping is even less.

For a sine wave input, the maximum signal amplitude is $\frac{\Delta}{2}$ and its average power is $\frac{\Delta^2}{8}$. This gives a peak signal-to-noise ratio (SNR) as

$$\frac{S^2}{N^2} = \frac{9}{16\pi^2}\left(\frac{f_s}{f_b}\right)^3 . \tag{5.12}$$

We can see that the peak SNR is only a function of the frequency ratio $\frac{f_s}{f_b}$. The faster the converter is sampled, the higher the resolution can be achieved. The expression in Eq. 5.12 can be transformed into

$$SNR = 10\log_{10}\frac{S^2}{N^2} = 20\log_{10}\left(\frac{3}{\sqrt{2}\pi}\right) + 9\log_2 M(dB) , \tag{5.13}$$

where M is an important parameter called the oversampling ratio, defined as the ratio of the sampling frequency over the Nyquist sampling frequency $2f_b$. From this expression, we can see that we can get $9\,dB$ of increase in SNR for every doubling of the sampling frequency. This corresponds to 1.5 bits. For example, if $M = 128$, we have 11.5 bits more resolution than sampling at the Nyquist rate. This method allows a high resolution A/D conversion by using only a one-bit quantizer.

We can see that higher resolution is achieved by trading off the input signal bandwidth. In order to get 1.5 more bits, the bandwidth has to be cut by a half in this structure. To have a more favorable resolution and bandwidth trade-off, we can go to higher order delta-sigma converters.

Higher-Order Single-Stage Converters

In the first-order delta-sigma converter, the noise-shaping function is $H_{ns}(z) = 1 - z^{-1}$. Higher order converters can allow the noise-shaping function go up to Lth power, given as

$$H_{ns}(z) = \left(1 - z^{-1}\right)^L , \tag{5.14}$$

where L is an integer greater than one. Thus, the magnitude of this noise-shaping function is

$$|H_{ns}(z)| = \left|\left(1 - z^{-1}\right)^L\right| = [2\sin(\pi f)]^L \ . \tag{5.15}$$

This function is also plotted in Fig. 5.16 for $L = 2$. As seen in the figure, more noise from the signal band is blocked than with the first-order function. Integrating Eq. 5.14 over the signal band allows calculation of the SNR of an Lth order delta-sigma converter as

$$\frac{S^2}{N^2} = \frac{3(2L+1)}{2^{2L+2} \cdot \pi^{2L}} \cdot \left(\frac{f_s}{f_b}\right)^{2L+1} \ , \tag{5.16}$$

which is equivalent to

$$SNR = 20\log_{10} = \left(\frac{\sqrt{3(2L+1)/2}}{\pi^L}\right) + 3(2L+1)\log_2 M(dB) \ , \tag{5.17}$$

where M is the oversampling ratio. For every doubling of the sampling frequency, the SNR is increased by $3(2L+1)dB$, i.e., $L + 0.5$ bits more resolution. For example, $L = 2$ adds 2.5 bits and

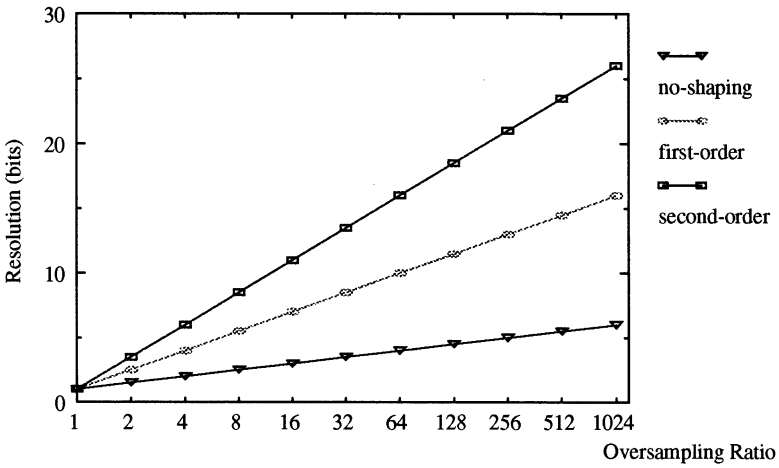

FIGURE 5.17: A plot of the resolution vs. oversampling ratio for different types of delta-sigma converters and Nyquist sampling converter.

$L = 3$ adds 3.5 bits of resolution. Therefore, compared to the first-order system, by employing a higher order delta-sigma converter architecture, the same resolution can be achieved with a lower sampling frequency, or a higher input bandwidth can be allowed at the same resolution with the same sampling frequency. Figure 5.17 shows a plot of Eq. 5.17 comparing resolution vs. oversampling ratio for different order delta-sigma converters.

A second-order delta-sigma converter can be realized as shown in Fig. 5.18 with two integrators. Higher order converters can be similarly constructed. However, when the order of the converter is greater than two, special care must be taken to insure the converter stability [9]. More zeroes are introduced in the transfer function of the forward path to suppress the signal swing after the integrators.

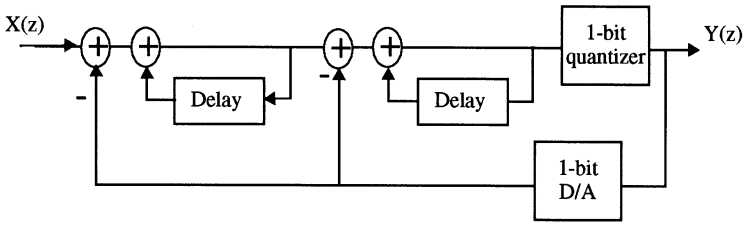

FIGURE 5.18: Block diagram of a second order D-S modulator.

Other methods can be used to improve the resolution of the delta-sigma converter. A first-order and a second-order converter can be cascaded to achieve the same performance as a third-order converter, but with better stability over the frequency range [10]. A multi-bit quantizer can also be used to replace the 1-bit quantizer in the architecture presented here [11]. This improves the resolution at the same sampling speed. Interested readers are referred to reference articles.

In an oversampling converter, the digital decimation filter is also an integral part. Only after the decimation filter is the resolution of the converter realized. The design of decimation filters are discussed in other sections of this book and can also be found in the reference article by Candy [12].

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