SECTION 3

ADCs FOR DSP APPLICATIONS

- Successive Approximation ADCs
- Sigma-Delta ADCs
- Flash Converters
- Subranging (Pipelined) ADCs
- Bit-Per-Stage (Serial, or Ripple) ADCs

SECTION 3

ADCs FOR DSP APPLICATIONS

Walt Kester, James Bryant

The trend in ADCs and DACs is toward higher speeds and higher resolutions at reduced power levels and supply voltages. Modern data converters generally operate on ±5V (dual supply), +5V or +3V (single supply). In fact, the number of +3V devices is rapidly increasing because of many new markets such as digital cameras, camcorders, and cellular telephones. This trend has created a number of design and applications problems which were much less important in earlier data converters, where ±15V supplies and ±10V input ranges were the standard.

Lower supply voltages imply smaller input voltage ranges, and hence more susceptibility to noise from all potential sources: power supplies, references, digital signals, EMI/RFI, and probably most important, improper layout, grounding, and decoupling techniques. Single-supply ADCs often have an input range which is not referenced to ground. Finding compatible single-supply drive amplifiers and dealing with level shifting of the input signal in direct-coupled applications also becomes a challenge.

In spite of these issues, components are now available which allow extremely high resolutions at low supply voltages and low power. This section discusses the applications problems associated with such components and shows techniques for successfully designing them into systems.

The most popular ADCs for DSP applications are based on five fundamental architectures: *successive approximation, sigma-delta, flash, subranging (or pipelined),* and *bit-per-stage (or ripple).*

LOW POWER, LOW VOLTAGE ADC DESIGN ISSUES

- **Typical Supply Voltages: ±5V, +5V, +5/+3V, +3V**
- **Lower Signal Swings Increase Sensitivity to**

  All Types of Noise (Device, Power Supply, Logic, etc.)
- **Device Noise Increases at Low Currents**
- **Common Mode Input Voltage Restrictions**
- **Input Buffer Amplifier Selection Critical**
- **Auto-Calibration Modes Desirable at High Resolutions**

Figure 3.1

ADCs FOR DSP APPLICATIONS

- **Successive Approximation**
  - **Resolutions to 16-bits**
  - **Minimal Throughput Delay Time (No Output Latency, "Single-Shot" Operation Possible**
  - **Used in Multiplexed Data Acquisition Systems**
- **Sigma-Delta**
  - **Resolutions to 24-bits**
  - **Excellent Differential Linearity**
  - **Internal Digital Filter (Can be Linear Phase)**
  - **Long Throughput Delay Time (Output Latency)**
  - **Difficult to Multiplex Inputs Due to Digital Filter Settling Time**
- **High Speed Architectures:**
  - **Flash Converter**
  - **Subranging or Pipelined**
  - **Bit-Per-Stage (Ripple)**

Figure 3.2

SUCCESSIVE APPROXIMATION ADCs

The successive approximation ADC has been the mainstay of signal conditioning for many years. Recent design improvements have extended the sampling frequency of these ADCs into the megahertz region. The use of internal switched capacitor techniques along with auto calibration techniques extend the resolution of these ADCs to 16-bits on standard CMOS processes without the need for expensive thin-film laser trimming.

The basic successive approximation ADC is shown in Figure 3.3. It performs conversions on command. On the assertion of the CONVERT START command, the sample-and-hold (SHA) is placed in the *hold* mode, and all the bits of the successive approximation register (SAR) are reset to "0" except the MSB which is set to "1". The SAR output drives the internal DAC. If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The next most significant bit is then set to "1". If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The process is repeated with each bit in turn. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete. These bit “tests” can form the basis of a serial output version SAR-based ADC.

The end of conversion is generally indicated by an end-of-convert (EOC), data-ready (DRDY), or a busy signal (actually, *not*-BUSY indicates end of conversion). The polarities and name of this signal may be different for different SAR ADCs, but the fundamental concept is the same. At the beginning of the conversion interval, the signal goes high (or low) and remains in that state until the conversion is completed, at which time it goes low (or high). The trailing edge is generally an indication of valid output data.

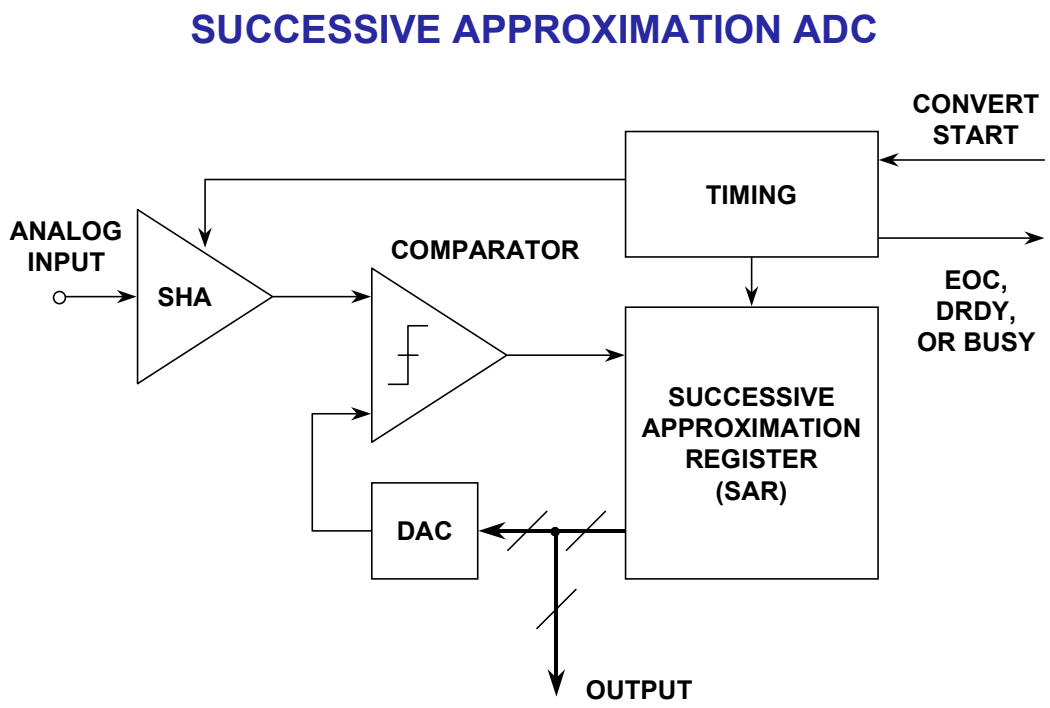


Figure 3.3

An N-bit conversion takes N steps. It would seem on superficial examination that a 16-bit converter would have twice the conversion time of an 8-bit one, but this is not the case. In an 8-bit converter, the DAC must settle to 8-bit accuracy before the bit decision is made, whereas in a 16-bit converter, it must settle to 16-bit accuracy, which takes a lot longer. In practice, 8-bit successive approximation ADCs can convert in a few hundred nanoseconds, while 16-bit ones will generally take several microseconds.

Notice that the overall accuracy and linearity of the SAR ADC is determined primarily by the internal DAC. Until recently, most precision SAR ADCs used laser-trimmed thin-film DACs to achieve the desired accuracy and linearity. The thin-film resistor trimming process adds cost, and the thin-film resistor values may be affected when subjected to the mechanical stresses of packaging.

For these reasons, switched capacitor (or charge-redistribution) DACs have become popular in newer SAR ADCs. The advantage of the switched capacitor DAC is that the accuracy and linearity is primarily determined by photolithography, which in turn controls the capacitor plate area and the capacitance as well as matching. In

addition, small capacitors can be placed in parallel with the main capacitors which can be switched in and out under control of autocalibration routines to achieve high accuracy and linearity without the need for thin-film laser trimming. Temperature tracking between the switched capacitors can be better than 1ppm/°C, thereby offering a high degree of temperature stability.

A simple 3-bit capacitor DAC is shown in Figure 3.4. The switches are shown in the *track*, or *sample* mode where the analog input voltage, A_{IN}, is constantly charging and discharging the parallel combination of all the capacitors. The *hold* mode is initiated by opening S_{IN}, leaving the sampled analog input voltage on the capacitor array. Switch S_C is then opened allowing the voltage at node A to move as the bit switches are manipulated. If S1, S2, S3, and S4 are all connected to ground, a voltage equal to $-A_{IN}$ appears at node A. Connecting S1 to V_{REF} adds a voltage equal to $V_{REF}/2$ to $-A_{IN}$. The comparator then makes the MSB bit decision, and the SAR either leaves S1 connected to V_{REF} or connects it to ground depending on the comparator output (which is high or low depending on whether the voltage at node A is negative or positive, respectively). A similar process is followed for the remaining two bits. At the end of the conversion interval, S1, S2, S3, S4, and S_{IN} are connected to A_{IN}, S_C is connected to ground, and the converter is ready for another cycle.

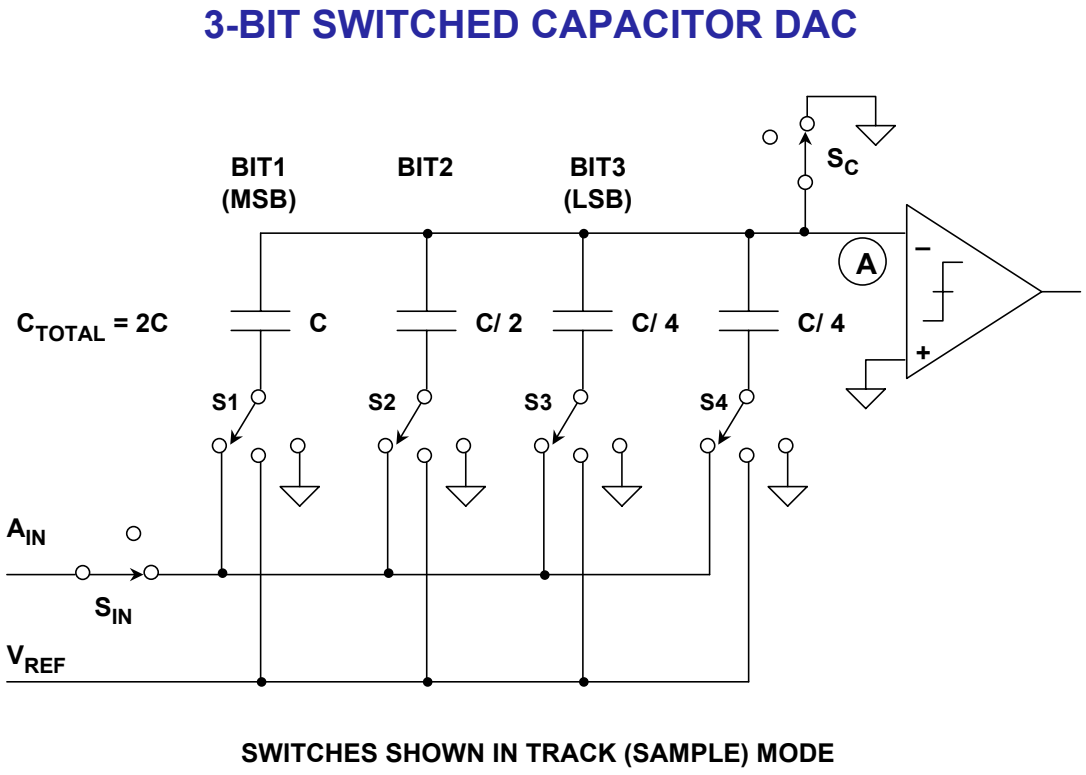


Figure 3.4

Note that the extra LSB capacitor (C/4 in the case of the 3-bit DAC) is required to make the total value of the capacitor array equal to 2C so that binary division is accomplished when the individual bit capacitors are manipulated.

The operation of the capacitor DAC (cap DAC) is similar to an R/2R resistive DAC. When a particular bit capacitor is switched to V_{REF}, the voltage divider created by the bit capacitor and the total array capacitance (2C) adds a voltage to node A equal to the weight of that bit. When the bit capacitor is switched to ground, the same voltage is subtracted from node A.

Because of their popularity, successive approximation ADCs are available in a wide variety of resolutions, sampling rates, input and output options, package styles, and costs. It would be impossible to attempt to list all types, but Figure 3.5 shows a number of recent Analog Devices' SAR ADCs which are representative. Note that many devices are complete data acquisition systems with input multiplexers which allow a single ADC core to process multiple analog channels.

RESOLUTION / CONVERSION TIME COMPARISON FOR REPRESENTATIVE SINGLE-SUPPLY SAR ADCs

	RESOLUTION	SAMPLING RATE	POWER	CHANNELS
AD7472	12-BITS	1.5MSPS	9mW	1
AD7891	12-BITS	500kSPS	85mW	8
AD7858/59	12-BITS	200kSPS	20mW	8
AD7887/88	12-BITS	125kSPS	3.5mW	8
AD7856/57	14-BITS	285kSPS	60mW	8
AD7660	16-BITS	100kSPS	15mW	1
AD974	16-BITS	200kSPS	120mW	4
AD7664	16-BITS	570kSPS	150mW	1

Figure 3.5

While there are some variations, the fundamental timing of most SAR ADCs is similar and relatively straightforward (see Figure 3.6). The conversion process is initiated by asserting a CONVERT START signal. The $\overline{\text{CONVST}}$ signal is a negative-going pulse whose positive-going edge actually initiates the conversion. The internal sample-and-hold (SHA) amplifier is placed in the hold mode on this edge, and the various bits are determined using the SAR algorithm. The negative-going edge of the $\overline{\text{CONVST}}$ pulse causes the $\overline{\text{EOC}}$ or BUSY line to go high. When the conversion is complete, the BUSY line goes low, indicating the completion of the conversion process. In most cases the trailing edge of the BUSY line can be used as an indication that the output data is valid and can be used to strobe the output data into an external register. However, because of the many variations in terminology

and design, the individual data sheet should always be consulted when using a specific ADC.

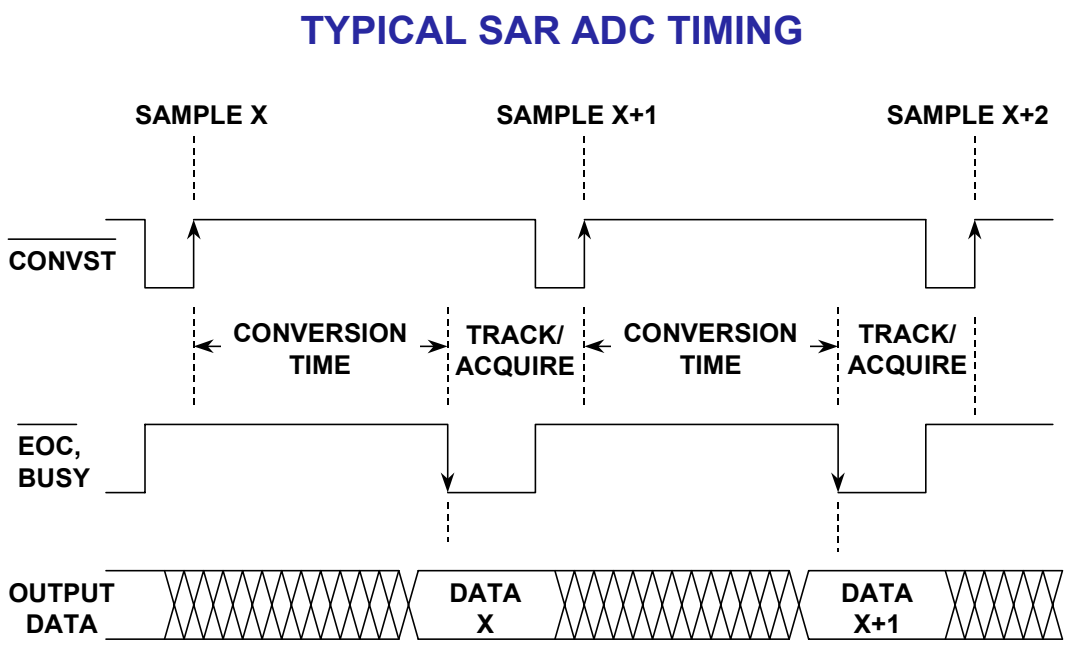


Figure 3.6

It should also be noted that some SAR ADCs require an external high frequency clock in addition to the CONVERT START command. In most cases, there is no need to synchronize the two. The frequency of the external clock, if required, generally falls in the range of 1MHz to 30MHz depending on the conversion time and resolution of the ADC. Other SAR ADCs have an internal oscillator which is used to perform the conversions and only require the CONVERT START command. Because of their architecture, SAR ADCs allow single-shot conversion at any repetition rate from DC to the converter's maximum conversion rate.

In a SAR ADC, the output data for a sampled input is valid at the end of the conversion interval for that sampled input. In other ADC architectures, such as sigma-delta or the two-stage subranging architecture shown in Figure 3.7, this is not the case. The subranging ADC shown in the figure is a two-stage *pipelined* or subranging 12-bit converter. The first conversion is done by the 6-bit ADC which drives a 6-bit DAC. The output of the 6-bit DAC represents a 6-bit approximation to the analog input. Note that SHA2 delays the analog signal while the 6-bit ADC makes its decision and the 6-bit DAC settles. The DAC approximation is then subtracted from the analog signal from SHA2, amplified, and digitized by a 7-bit ADC. The outputs of the two conversions are combined, and the extra bit used to correct errors made in the first conversion. The typical timing associated with this type of converter is shown in Figure 3.8. Note that the output data presented immediately after sample X actually corresponds to sample X–2, i.e., there is a two clock-cycle "pipeline" delay. The pipelined ADC architecture is generally associated with high speed ADCs, and in most cases the pipeline delay, or *latency*, is not a major system problem in most applications where this type of converter is used.

12-BIT TWO-STAGE PIPELINED ADC ARCHITECTURE

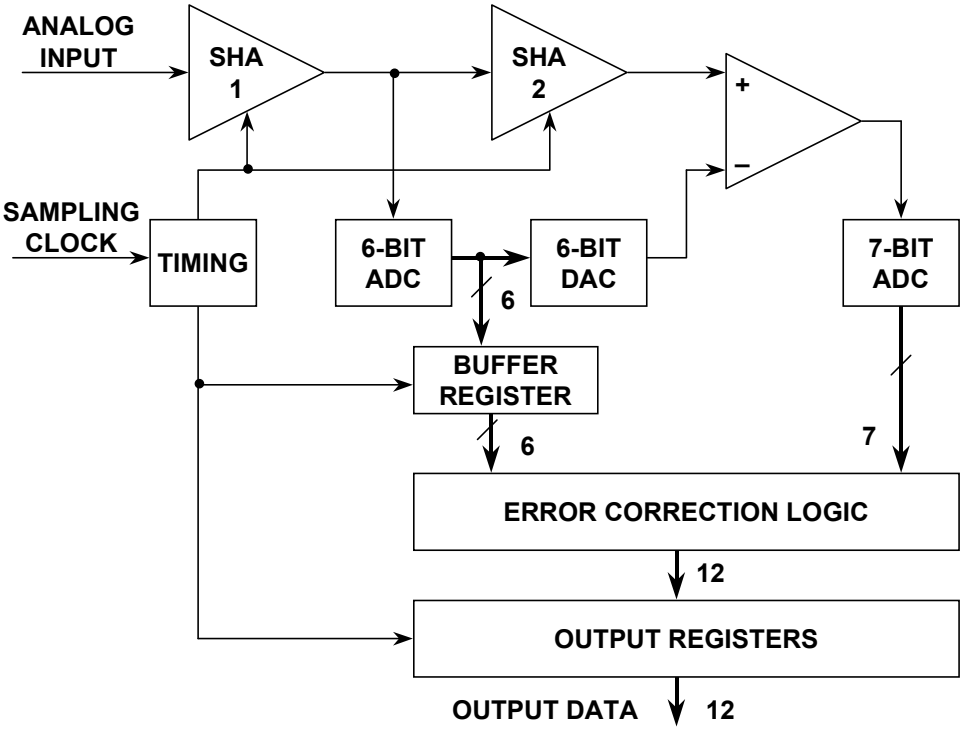
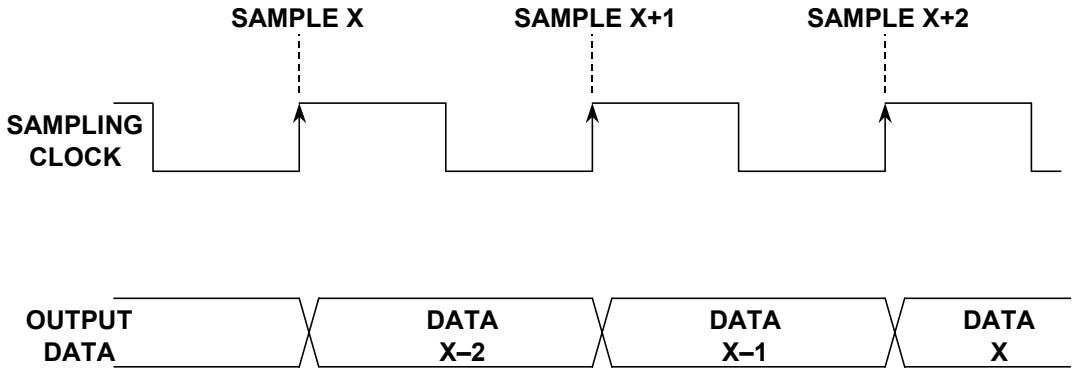


Figure 3.7

TYPICAL PIPELINED ADC TIMING



ABOVE SHOWS TWO CLOCK-CYCLES PIPELINE DELAY

Figure 3.8

Pipelined ADCs may have more than two clock-cycles latency depending on the particular architecture. For instance, the conversion could be done in three, or four, or perhaps even more pipelined stages causing additional latency in the output data.

Therefore, if the ADC is to be used in an event-triggered (or single-shot) mode where there must be a one-to-one time correspondence between each sample and the corresponding data, then the pipeline delay can be troublesome, and the SAR architecture is advantageous. Pipeline delay or latency can also be a problem in high speed servo-loop control systems or multiplexed applications. In addition, some pipelined converters have a *minimum* allowable conversion rate and must be kept running to prevent saturation of internal nodes.

Switched capacitor SAR ADCs generally have unbuffered input circuits similar to the circuit shown in Figure 3.9 for the AD7858/59 ADC. During the acquisition time, the analog input must charge the 20pF equivalent input capacitance to the correct value. If the input is a DC signal, then the source resistance, R_S, in series with the 125Ω internal switch resistance creates a time constant. In order to settle to 12-bit accuracy, approximately 9 time constants must be allowed for settling, and this defines the minimum allowable acquisition time. (Settling to 14-bits requires about 10 time constants, and 16-bits requires about 11).

$$t_{ACQ} > 9 \times (R_S + 125)\Omega \times 20\text{pF}.$$

For example, if $R_S = 50\Omega$, the acquisition time per the above formula must be at least 310ns.

For AC applications, a low impedance source should be used to prevent distortion due to the non-linear ADC input circuit. In a single supply application, a fast settling rail-to-rail op amp such as the AD820 should be used. Fast settling allows the op amp to settle quickly from the transient currents induced on its input by the internal ADC switches. In Figure 3.9, the AD820 drives a lowpass filter consisting of the 50Ω series resistor and the 10nF capacitor (cutoff frequency approximately 320kHz). This filter removes high frequency components which could result in aliasing and decreases the noise.

Using a single supply op amp in this application requires special consideration of signal levels. The AD820 is connected in the inverting mode and has a signal gain of –1. The noninverting input is biased at a common mode voltage of +1.3V with the 10.7kΩ/10kΩ divider, resulting in an output voltage of +2.6V for V_{IN}= 0V, and +0.1V for V_{IN} = +2.5V. This offset is provided because the AD820 output cannot go all the way to ground, but is limited to the V_{CESAT} of the output stage NPN transistor, which under these loading conditions is about 50mV. The input range of the ADC is also offset by +100mV by applying the +100mV offset from the 412Ω/10kΩ divider to the AIN– input.

DRIVING SWITCHED CAPACITOR INPUTS OF AD7858/59 12-BIT, 200kSPS ADC

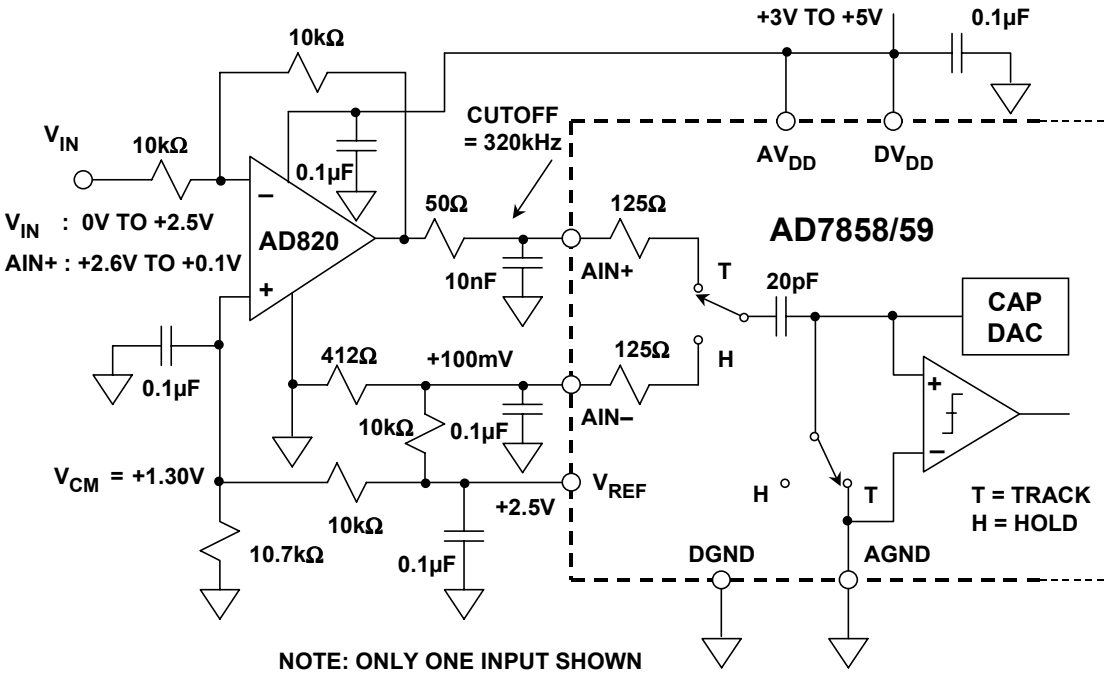


Figure 3.9

SIGMA-DELTA (ΣΔ) ADCS

James M. Bryant

Sigma-Delta Analog-Digital Converters (ΣΔ ADCs) have been known for nearly thirty years, but only recently has the technology (high-density digital VLSI) existed to manufacture them as inexpensive monolithic integrated circuits. They are now used in many applications where a low-cost, low-bandwidth, low-power, high-resolution ADC is required.

There have been innumerable descriptions of the architecture and theory of ΣΔ ADCs, but most commence with a maze of integrals and deteriorate from there. In the Applications Department at Analog Devices, we frequently encounter engineers who do not understand the theory of operation of ΣΔ ADCs and are convinced, from study of a typical published article, that it is too complex to comprehend easily.

There is nothing particularly difficult to understand about ΣΔ ADCs, as long as you avoid the detailed mathematics, and this section has been written in an attempt to clarify the subject. A ΣΔ ADC contains very simple analog electronics (a comparator, voltage reference, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. This circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably,

a low pass filter). It is not necessary to know precisely how the filter works to appreciate what it does. To understand how a ΣΔ ADC works, familiarity with the concepts of *over-sampling, quantization noise shaping, digital filtering,* and *decimation* is required.

SIGMA-DELTA ADCs

- **Low Cost, High Resolution (to 24-bits)**
- **Excellent DNL**
- **Low Power, but Limited Bandwidth (Voiceband, Audio)**
- **Key Concepts are Simple, but Math is Complex**
  - **Oversampling**
  - **Quantization Noise Shaping**
  - **Digital Filtering**
  - **Decimation**
- **Ideal for Sensor Signal Conditioning**
  - **High Resolution**
  - **Self, System, and Auto Calibration Modes**
- **Wide Applications in Voiceband and Audio Signal Processing**

Figure 3.10

Let us consider the technique of over-sampling with an analysis in the frequency domain. Where a DC conversion has a *quantization error* of up to ½ LSB, a sampled data system has *quantization noise*. A perfect classical N-bit sampling ADC has an RMS quantization noise of $q/\sqrt{12}$ uniformly distributed within the Nyquist band of DC to $f_S/2$ (where q is the value of an LSB and f_S is the sampling rate) as shown in Figure 3.11A. Therefore, its SNR with a full-scale sinewave input will be (6.02N + 1.76) dB. If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantization noise, then its *effective* resolution will be less than N-bits. Its actual resolution (often known as its Effective Number of Bits or ENOB) will be defined by

$$\text{ENOB} = \frac{\text{SNR} - 1.76\text{dB}}{6.02\text{dB}}.$$

If we choose a much higher sampling rate, Kf_S (see Figure 3.11B), the RMS quantization noise remains $q/\sqrt{12}$, but the noise is now distributed over a wider bandwidth DC to $Kf_S/2$. If we then apply a digital low pass filter (LPF) to the output, we remove much of the quantization noise, but do not affect the wanted

signal - so the ENOB is improved. We have accomplished a high resolution A/D conversion with a low resolution ADC. The factor K is generally referred to as the *oversampling ratio*. It should be noted at this point that oversampling has an added benefit in that it relaxes the requirements on the analog antialiasing filter.

OVERSAMPLING, DIGITAL FILTERING, NOISE SHAPING, AND DECIMATION

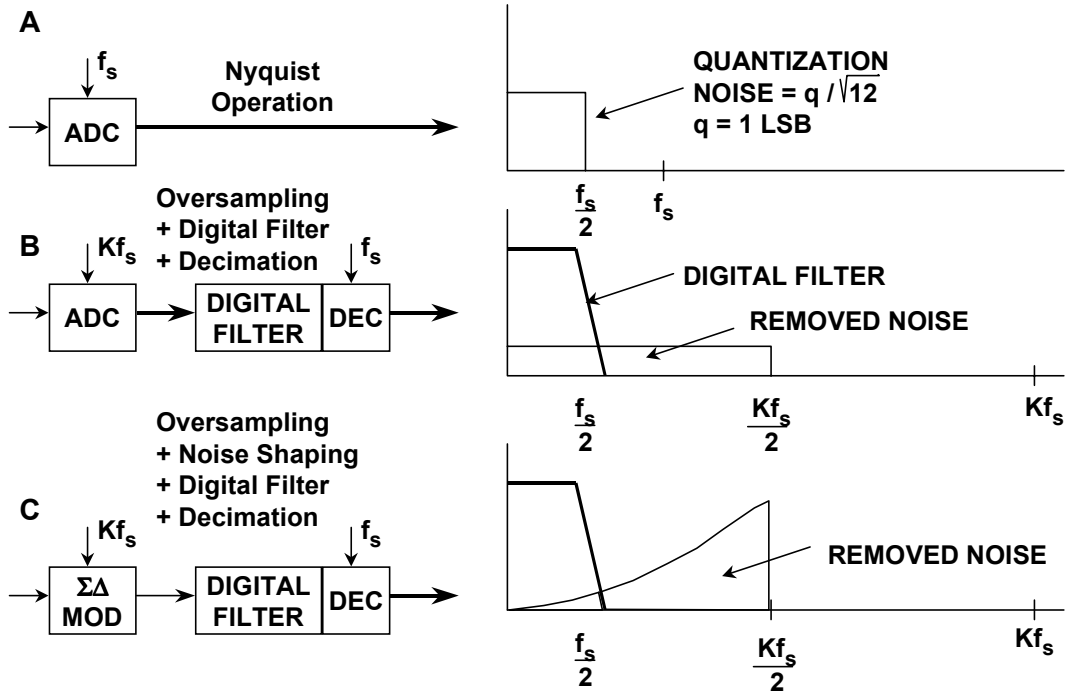


Figure 3.11

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate (Kf_S) and still satisfy the Nyquist criterion. This may be achieved by passing every Mth result to the output and discarding the remainder. The process is known as "decimation" by a factor of M. Despite the origins of the term (*decem* is Latin for ten), M can have any integer value, provided that the output data rate is more than twice the signal bandwidth. Decimation does not cause any loss of information (see Figure 3.11B).

If we simply use over-sampling to improve resolution, we must over-sample by a factor of 2^{2N} to obtain an N-bit increase in resolution. The ΣΔ converter does not need such a high over-sampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband as shown in Figure 3.11C.

If we take a 1-bit ADC (generally known as a comparator), drive it with the output of an integrator, and feed the integrator with an input signal summed with the output of a 1-bit DAC fed from the ADC output, we have a first-order ΣΔ modulator as shown in Figure 3.12. Add a digital low pass filter (LPF) and decimator at the digital output, and we have a ΣΔ ADC: the ΣΔ modulator shapes the quantization

noise so that it lies above the passband of the digital output filter, and the ENOB is therefore much larger than would otherwise be expected from the over-sampling ratio.

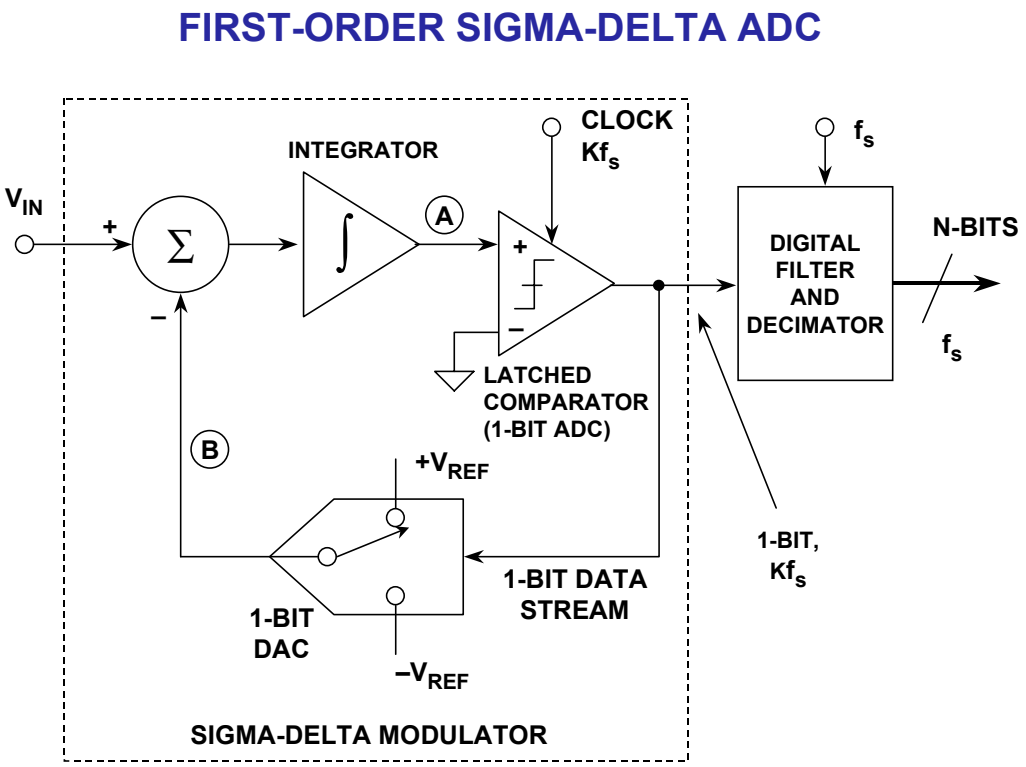


Figure 3.12

Intuitively, a ΣΔ ADC operates as follows. Assume a DC input at V_{IN}. The integrator is constantly ramping up or down at node A. The output of the comparator is fed back through a 1-bit DAC to the summing input at node B. The negative feedback loop from the comparator output through the 1-bit DAC back to the summing point will force the average DC voltage at node B to be equal to V_{IN}. This implies that the average DAC output voltage must equal to the input voltage V_{IN}. The average DAC output voltage is controlled by the *ones-density* in the 1-bit data stream from the comparator output. As the input signal increases towards $+V_{REF}$, the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. Similarly, as the signal goes negative towards $-V_{REF}$, the number of "ones" in the serial bit stream decreases, and the number of "zeros" increases. From a very simplistic standpoint, this analysis shows that the average value of the input voltage is contained in the serial bit stream out of the comparator. The digital filter and decimator process the serial bit stream and produce the final output data.

The concept of noise shaping is best explained in the frequency domain by considering the simple ΣΔ modulator model in Figure 3.13.

SIMPLIFIED FREQUENCY DOMAIN LINEARIZED MODEL OF A SIGMA-DELTA MODULATOR

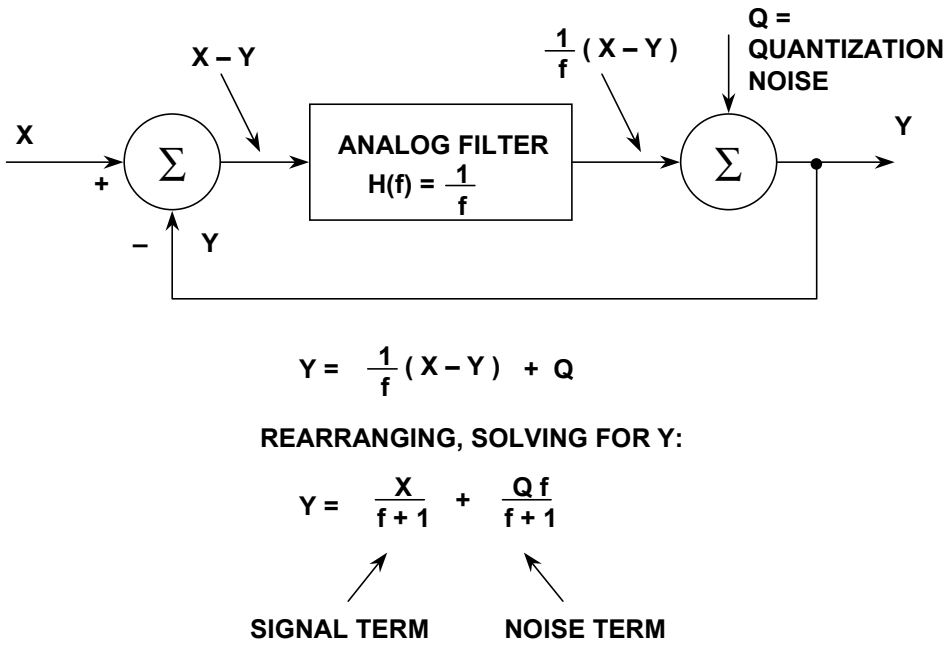


Figure 3.13

The integrator in the modulator is represented as an analog lowpass filter with a transfer function equal to H(f) = 1/f. This transfer function has an amplitude response which is inversely proportional to the input frequency. The 1-bit quantizer generates quantization noise, Q, which is injected into the output summing block. If we let the input signal be X, and the output Y, the signal coming out of the input summer must be X – Y. This is multiplied by the filter transfer function, 1/f, and the result goes to one input to the output summer. By inspection, we can then write the expression for the output voltage Y as:

$$Y = \frac{1}{f}(X - Y) + Q.$$

This expression can easily be rearranged and solved for Y in terms of X, f, and Q:

$$Y = \frac{X}{f+1} + \frac{Q \cdot f}{f+1}.$$

Note that as the frequency f approaches zero, the output voltage Y approaches X with no noise component. At higher frequencies, the amplitude of the signal component approaches zero, and the noise component approaches Q. At high frequency, the output consists primarily of quantization noise. In essence, the analog filter has a lowpass effect on the signal, and a highpass effect on the quantization noise. Thus the analog filter performs the noise shaping function in the ΣΔ modulator model.

For a given input frequency, higher order analog filters offer more attenuation. The same is true of ΣΔ modulators, provided certain precautions are taken.

By using more than one integration and summing stage in the ΣΔ modulator, we can achieve higher orders of quantization noise shaping and even better ENOB for a given over-sampling ratio as is shown in Figure 3.14 for both a first and second-order ΣΔ modulator. The block diagram for the second-order ΣΔ modulator is shown in Figure 3.15. Third, and higher, order ΣΔ ADCs were once thought to be potentially unstable at some values of input - recent analyses using *finite* rather than infinite gains in the comparator have shown that this is not necessarily so, but even if instability does start to occur, it is not important, since the DSP in the digital filter and decimator can be made to recognize incipient instability and react to prevent it.

Figure 3.16 shows the relationship between the order of the ΣΔ modulator and the amount of over-sampling necessary to achieve a particular SNR. For instance, if the oversampling ratio is 64, an ideal second-order system is capable of providing an SNR of about 80dB. This implies approximately 13 effective number of bits (ENOB). Although the filtering done by the digital filter and decimator can be done to any degree of precision desirable, it would be pointless to carry more than 13 binary bits to the outside world. Additional bits would carry no useful signal information, and would be buried in the quantization noise unless post-filtering techniques were employed. Additional resolution can be obtained by increasing the oversampling ratio and/or by using a higher-order modulator.

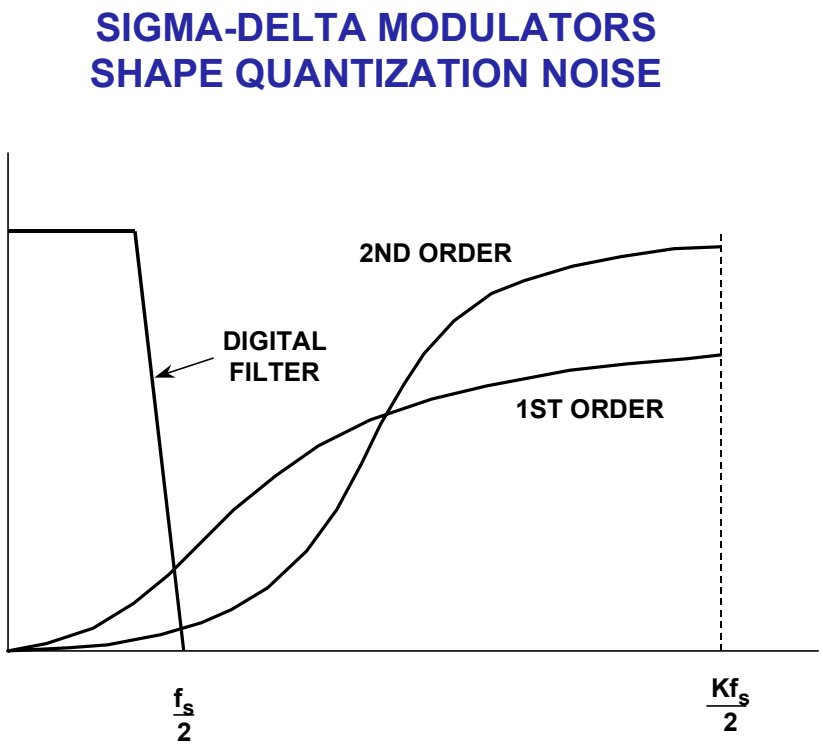


Figure 3.14

SECOND-ORDER SIGMA-DELTA ADC

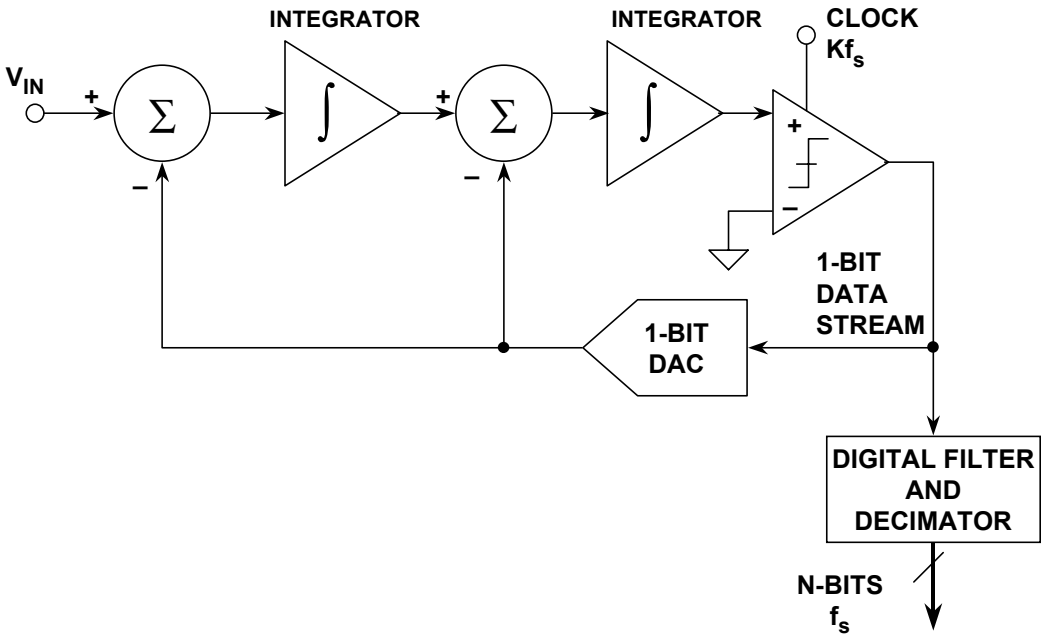


Figure 3.15

SNR VERSUS OVERSAMPLING RATIO FOR FIRST, SECOND, AND THIRD-ORDER LOOPS

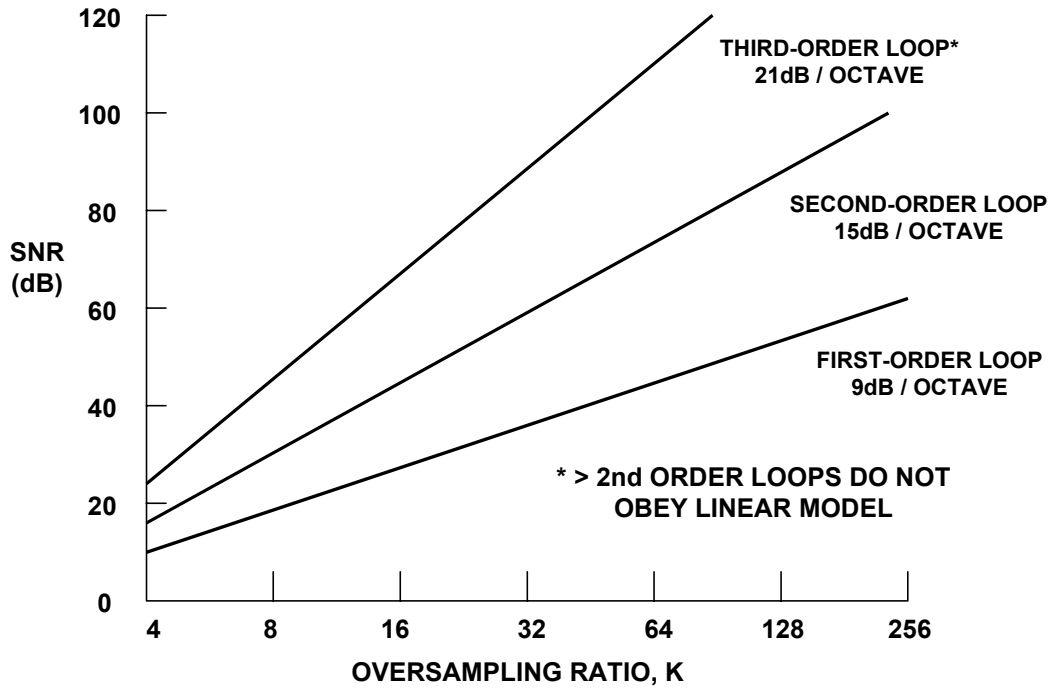


Figure 3.16

The AD1877 is a 16-bit 48kSPS stereo sigma-delta DAC suitable for demanding audio applications. Key specifications are summarized in Figure 3.17. This device has a 64X oversampling ratio, and a fourth-order modulator. The internal digital filter is a linear phase FIR filter whose response is shown in Figure 3.18. The passband ripple is 0.006dB, and the attenuation is greater than 90dB in the stopband. The width of the transition region from passband to stopband is only $0.1f_S$, where f_S is the effective sampling frequency of the AD1877 (maximum of 48kSPS). Such a filter would obviously be impossible to implement in analog form.

AD1877 16-BIT, 48kSPS STEREO SIGMA-DELTA ADC

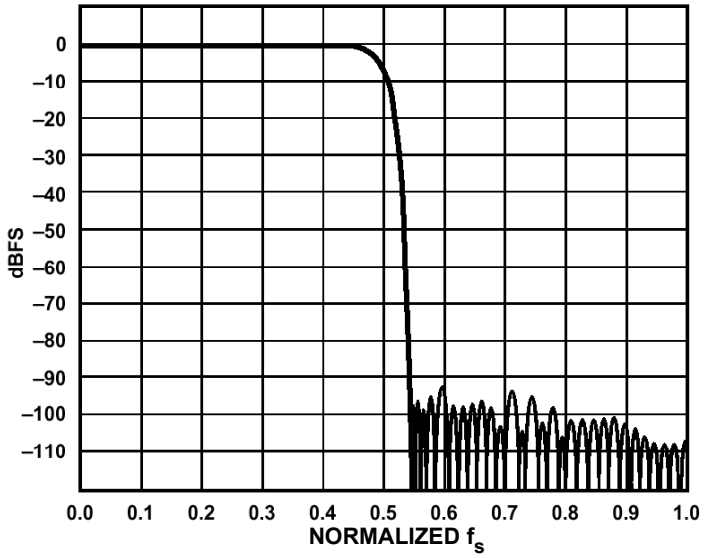
- **Single +5 V Power Supply**
- **Single-Ended Dual-Channel Analog Inputs**
- **92 dB (typ) Dynamic Range**
- **90 dB (typ) S/(THD+N)**
- **0.006 dB Decimator Passband Ripple**
- **Fourth-Order, 64-Times Oversampling ΣΔ Modulator**
- **Three-Stage, Linear-Phase Decimator**
- **Less than 100 mW (typ)**
- **Power-Down Mode**
- **Input Overrange Indication**
- **On-Chip Voltage Reference**
- **Flexible Serial Output Interface**
- **28-Pin SOIC Package**

Figure 3.17

All sigma-delta ADCs have a settling time associated with the internal digital filter, and there is no way to remove it. In multiplexed applications the input to the ADC is a step function if there are different input voltages on adjacent channels. In fact, the multiplexer output can represent a fullscale step voltage to the sigma-delta ADC when channels are switched. Adequate filter settling time must be allowed, therefore, in such applications. This does not mean that sigma-delta ADCs shouldn't be used in multiplexed applications, just that the settling time of the digital filter must be considered.

For example, the group delay through the AD1877 FIR filter is $36/f_S$, and represents the time it takes for a step function input to propagate through one-half the number of taps in the digital filter. The total time required for settling is therefore $72f_S$, or approximately 1.5ms when sampling at 48kSPS with a 64X oversampling rate.

AD1877 16-BIT, 48kSPS STEREO SIGMA-DELTA ADC FIR FILTER CHARACTERISTICS



- f_S = OUTPUT WORD RATE, 32kSPS, 44.1kSPS, OR 48kSPS TYPICAL
- PASSBAND TO STOPBAND TRANSITION REGION: $0.45f_S$ TO $0.55f_S$
- SETTLING TIME = 72 / f_S = 1.5ms FOR f_S = 48kSPS
- GROUP DELAY = 36 / f_S = 0.75ms FOR f_S = 48kSPS

Figure 3.18

In other applications, such as low frequency, high resolution 24-bit measurement sigma-delta ADCs (such as the AD77xx-series), other types of digital filters may be used. For instance, the $SINC^3$ response is popular because it has zeros at multiples of the throughput rate. For instance a 10Hz throughput rate produces zeros at 50Hz and 60Hz which aid in AC power line rejection.

So far we have considered only sigma-delta converters which contain a single-bit ADC (comparator) and a single-bit DAC (switch). The block diagram of Figure 3.19 shows a multi-bit sigma-delta ADC which uses an n-bit flash ADC and an n-bit DAC. Obviously, this architecture will give a higher dynamic range for a given oversampling ratio and order of loop filter. Stabilization is easier, since second-order and higher loops can be used. Idling patterns tend to be more random thereby minimizing tonal effects.

The real disadvantage of this technique is that the linearity depends on the DAC linearity, and thin film laser trimming is generally required to approach 16-bit performance levels. This makes the multi-bit architecture extremely difficult to implement on sigma-delta ADCs. It is, however, currently used in sigma-delta audio DACs (AD1852, AD1853, AD1854) where special "bit scrambling" techniques are used to ensure linearity and eliminate idle tones.

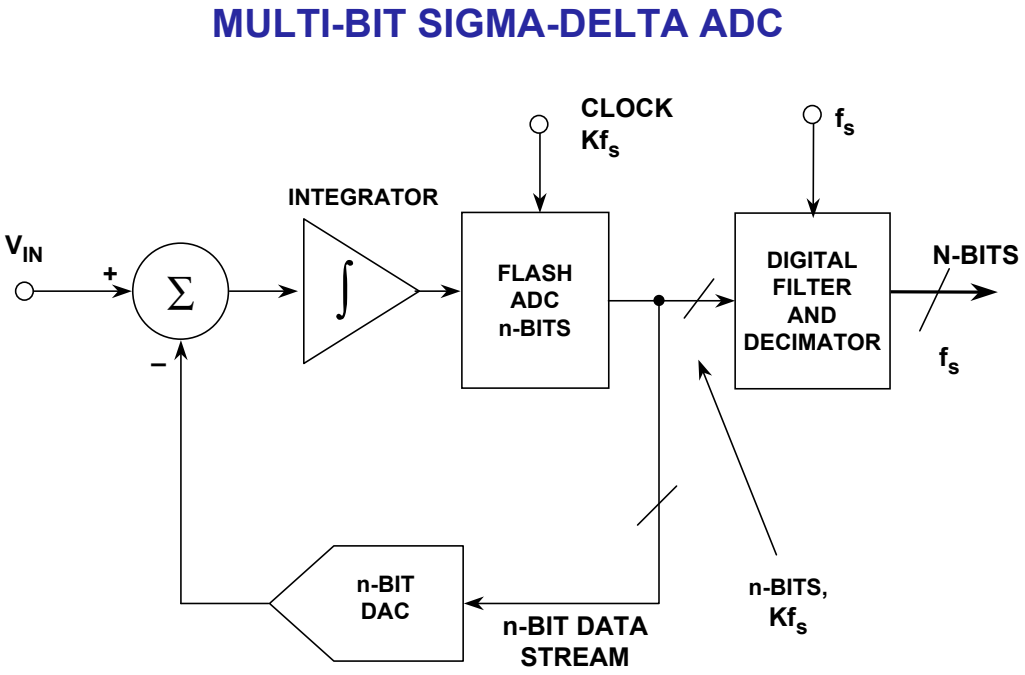


Figure 3.19

The ΣΔ ADCs that we have described so far contain integrators, which are low pass filters, whose passband extends from DC. Thus, their quantization noise is pushed up in frequency. At present, most commercially available ΣΔ ADCs are of this type (although some which are intended for use in audio or telecommunications applications contain bandpass rather than lowpass digital filters to eliminate any system DC offsets). But there is no particular reason why the filters of the ΣΔ modulator should be LPFs, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a ΣΔ ADC with bandpass filters (BPFs) as shown in Figure 3.20, the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the pass-band (see Reference 1). If the digital filter is then programmed to have its pass-band in this region, we have a ΣΔ ADC with a bandpass, rather than a lowpass characteristic. Such devices would appear to be useful in direct IF-to-digital conversion, digital radios, ultrasound, and other undersampling applications. However, the modulator and the digital BPF must be designed for the specific set of frequencies required by the system application, thereby somewhat limiting the flexibility of this approach.

In an undersampling application of a bandpass ΣΔ ADC, the minimum sampling frequency must be at least twice the signal bandwidth, BW. The signal is centered around a carrier frequency, f_c. A typical digital radio application using a 455kHz center frequency and a signal bandwidth of 10kHz is described in Reference 1. An oversampling frequency Kf_S = 2MSPS and an output rate f_S = 20kSPS yielded a dynamic range of 70dB within the signal bandwidth.

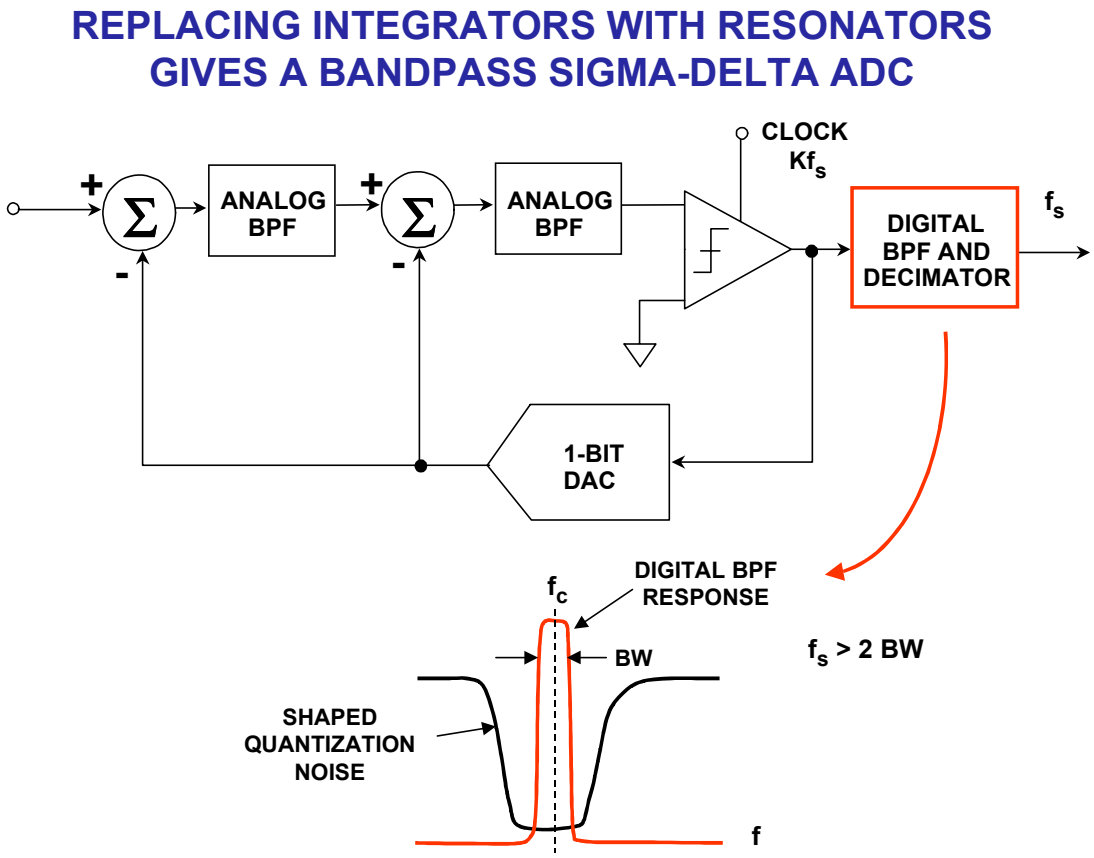


Figure 3.20

Most sigma-delta ADCs generally have a fixed internal digital filter. The filter's cutoff frequency and the ADC output data rate scales with the master clock frequency. The AD7725 is a 16-bit sigma-delta ADC with a programmable internal digital filter. The modulator operates at a maximum oversampling rate of 19.2MSPS. The modulator is followed by a preset FIR filter which decimates the modulator output by a factor of 8, yielding an output data rate of 2.4MSPS. The output of the preset filter drives a programmable FIR filter. By loading the ROM with suitable coefficient values, this filter can be programmed for the desired frequency response.

The programmable filter is flexible with respect to number of taps and decimation rate. The filter can have up to 108 taps, up to 5 decimation stages, and a decimation factor between 2 and 256. Coefficient precision is 24-bits, and arithmetic precision is 30-bits.

The AD7725 contains Systolix's PuldeDSP™ (trademark of Systolix) post processor which permits the filter characteristics to be programmed through the parallel or serial microprocessor interface. Or, it may boot at power-on-reset from its internal ROM or from an external EPROM.

The post processor is a fully programmable core which provides processing power of up to 130 million multiply-accumulates (MAC) per second. To program the post processor, the user must produce a configuration file which contains the programming data for the filter function. This file is generated by a compiler which is available from Analog Devices. The AD7725 compiler accepts filter coefficient data as an input and automatically generates the required device programming data.

The coefficient file for the FIR filter response can be generated using a digital filter design package such as QEDesign from Momentum Data Systems. The response of the filter can be plotted so the user knows the response before generating the filter coefficients. The data is available to the processor at a 2.4MSPS rate. When decimation is employed in a multistage filter, the first filter will be operated at 2.4MSPS, and the user can then decimate between stages. The number of taps which can be contained in the processor is 108. Therefore, a single filter with 108 taps can be generated, or a multistage filter can be designed whereby the total number of taps adds up to 108. The filter characteristic can be lowpass, highpass, bandstop, or bandpass.

The AD7725 operates on a single +5V supply, has an on-chip 2.5V reference, and is packaged in a 44-pin PQFP. Power dissipation is approximately 350mW when operating at full power. A half-power mode is available with a master clock frequency of 10MSPS maximum. Power consumption in the standby mode is 200mW maximum. More details of the AD7725 operation can be found in Section 9.

Summary

A ΣΔ ADC works by over-sampling, where simple analog filters in the ΣΔ modulator shape the quantization noise so that the SNR *in the bandwidth of interest* is much greater than would otherwise be the case, and by using high performance digital filters and decimation to eliminate noise outside the required passband. Oversampling has the added benefit of relaxing the requirements on the antialiasing filter. Because the analog circuitry is relatively undemanding, it may be built with the same digital VLSI process that is used to fabricate the DSP circuitry of the digital filter. Because the basic ADC is 1-bit (a comparator), the technique is inherently linear.

Although the detailed analysis of ΣΔ ADCs involves quite complex mathematics, their basic design can be understood without the necessity of any mathematics at all. For further discussion on ΣΔ ADCs, refer to References 1 through 18 at the end of this section.

SIGMA-DELTA SUMMARY

- **Inherently Excellent Linearity**
- **Oversampling Relaxes Analog Antialiasing Filter Requirements**
- **Ideal for Mixed-Signal IC Processes, no Trimming**
- **No SHA Required**
- **Added Functionality: On-Chip PGAs, Analog Filters, Autocalibration**
- **On-Chip Programmable Digital Filters (AD7725: Lowpass, Highpass, Bandpass, Bandstop)**
- **Upper Sampling Rate Currently Limits Applications to Measurement, Voiceband, and Audio, but Bandpass Sigma-Delta Techniques May Change This**
- **Analog Multiplexer Switching Speed Limited by Internal Filter Settling Time. Consider One Sigma-Delta ADC per Channel.**

Figure 3.21

FLASH CONVERTERS

Flash ADCs (sometimes called *parallel* ADCs) are the fastest type of ADC and use large numbers of comparators. An N-bit flash ADC consists of 2^N resistors and $2^N–1$ comparators arranged as in Figure 3.22. Each comparator has a reference voltage which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a "0" logic output. The $2^N–1$ comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a *thermometer* code. Since $2^N–1$ data outputs are not really practical, they are processed by a decoder to an N-bit binary output.

The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast. However, the architecture uses large numbers of resistors and comparators and is limited to low resolutions, and if it is to be fast, each comparator must run at relatively high power levels. Hence, the problems of flash ADCs include limited resolution, high power dissipation because of the large number of high speed comparators (especially at sampling rates greater than 50MSPS), and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators, so the voltage reference has to source quite large currents (>10 mA).

In practice, flash converters are available up to 10-bits, but more commonly they have 8-bits of resolution. Their maximum sampling rate can be as high as 1GHz, with input full-power bandwidths in excess of 300 MHz.

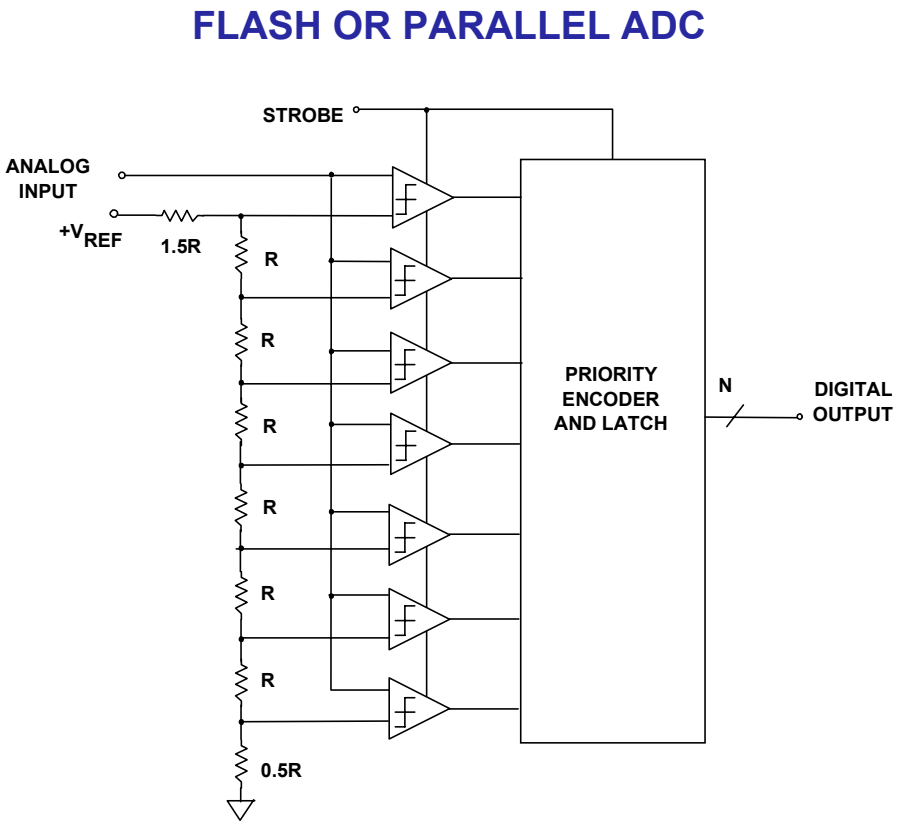


Figure 3.22

But as mentioned earlier, full-power bandwidths are not necessarily full-resolution bandwidths. Ideally, the comparators in a flash converter are well matched both for DC and AC characteristics. Because the strobe is applied to all the comparators simultaneously, the flash converter is inherently a sampling converter. In practice, there are delay variations between the comparators and other AC mismatches which cause a degradation in ENOB at high input frequencies. This is because the inputs are slewing at a rate comparable to the comparator conversion time.

The input to a flash ADC is applied in parallel to a large number of comparators. Each has a voltage-variable junction capacitance, and this signal-dependent capacitance results in most flash ADCs having reduced ENOB and higher distortion at high input frequencies.

Adding 1 bit to the total resolution of a flash converter requires doubling the number of comparators! This limits the practical resolution of high speed flash converters to 8-bits because of excessive power dissipation.

However, in the AD9410 10-bit, 200MSPS ADC, a technique called *interpolation* is used to minimize the number of preamplifiers in the flash converter comparators and also reduce the power (1.8W). The method is shown in Figure 3.23.

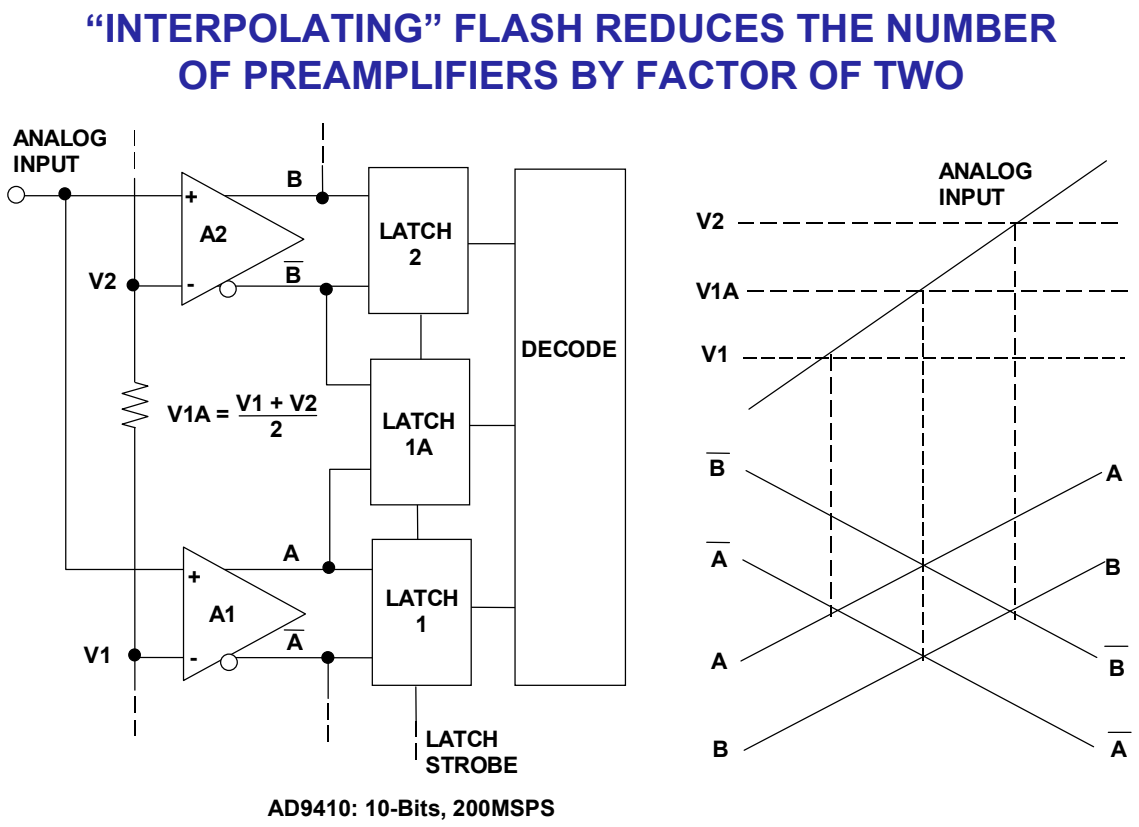


Figure 3.23

The preamplifiers (labeled "A1", "A2", etc.) are low-gain g_m stages whose bandwidth is proportional to the tail currents of the differential pairs. Consider the case for a positive-going ramp input which is initially below the reference to AMP A1, V1. As the input signal approaches V1, the differential output of A1 approaches zero (i.e., A = $\overline{A}$), and the decision point is reached. The output of A1 drives the differential input of LATCH 1. As the input signals continues to go positive, A continues to go positive, and $\overline{B}$ begins to go negative. The interpolated decision point is determined when A = $\overline{B}$. As the input continues positive, the third decision point is reached when B = $\overline{B}$. This novel architecture reduces the ADC input capacitance and thereby minimizes its change with signal level and the associated distortion. The AD9410 also uses an input sample-and-hold circuit for improved AC linearity.

SUBRANGING (PIPELINED) ADCS

Although it is not practical to make flash ADCs with high resolution (greater than 10-bits), flash ADCs are often used as subsystems in "subranging" ADCs (sometimes known as "half-flash ADCs"), which are capable of much higher resolutions (up to 16-bits).

A block diagram of an 8-bit subranging ADC based upon two 4-bit flash converters is shown in Figure 3.24. Although 8-bit flash converters are readily available at high sampling rates, this example will be used to illustrate the theory. The conversion process is done in two steps. The first four significant bits (MSBs) are digitized by the first flash (to better than 8-bits accuracy), and the 4-bit binary output is applied to a 4-bit DAC (again, better than 8-bit accurate). The DAC output is subtracted from the held analog input, and the resulting residue signal is amplified and applied to the second 4-bit flash. The outputs of the two 4-bit flash converters are then combined into a single 8-bit binary output word. If the residue signal range does not exactly fill the range of the second flash converter, non-linearities and perhaps missing codes will result.

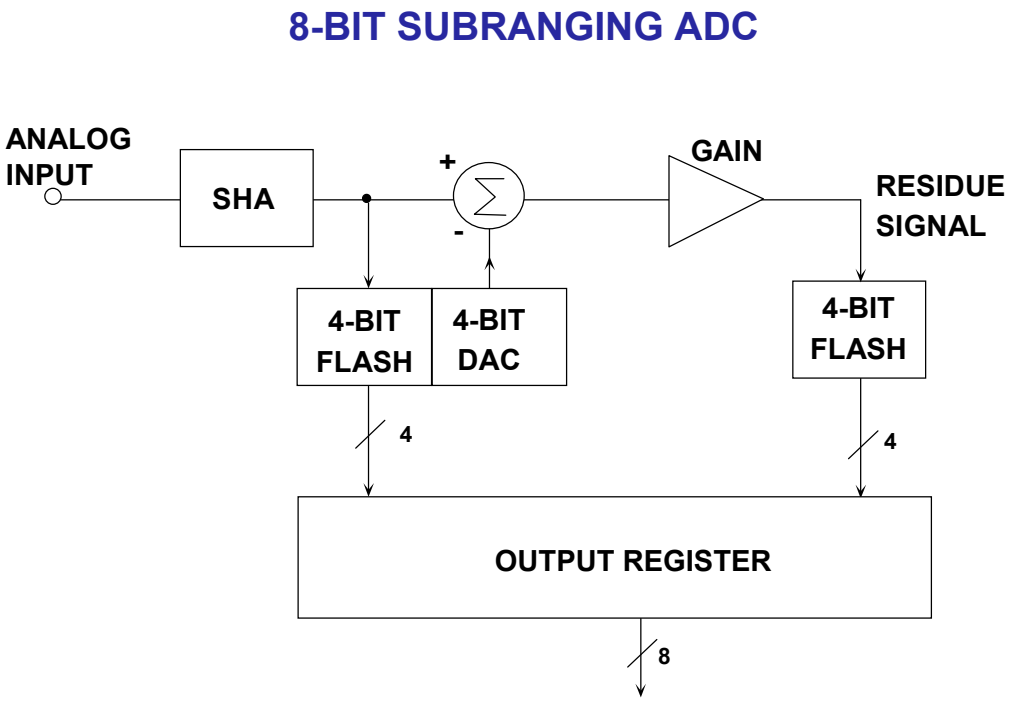


Figure 3.24

Modern subranging ADCs use a technique called *digital correction* to eliminate problems associated with the architecture of Figure 3.24. A simplified block diagram of a 12-bit digitally corrected subranging (DCS) ADC is shown in Figure 3.25. The architecture is similar to that used in the AD6640 12-bit, 65MSPS ADC. Note that a 6-bit and an 7-bit ADC have been used to achieve an overall 12-bit output. These are not flash ADCs, but utilize a *magnitude-amplifier (MagAmp™)* architecture which will be described shortly.

If there were no errors in the first-stage conversion, the 6-bit "residue" signal applied to the 7-bit ADC by the summing amplifier would never exceed one-half of the range of the 7-bit ADC. The extra range in the second ADC is used in conjunction with the error correction logic (usually just a full adder) to correct the output data for most of the errors inherent in the traditional uncorrected subranging converter architecture. It is important to note that the 6-bit DAC must

be better than 12-bit accurate, because the digital error correction does not correct for DAC errors. In practice, "thermometer" or "fully-decoded" DACs using one current switch per level (63 switches in the case of a 6-bit DAC) are often used instead of a "binary" DAC to ensure excellent differential and integral linearity and minimum switching transients.

AD6640 12-BIT, 65MSPS PIPELINED SUBRANGING ADC WITH DIGITAL ERROR CORRECTION

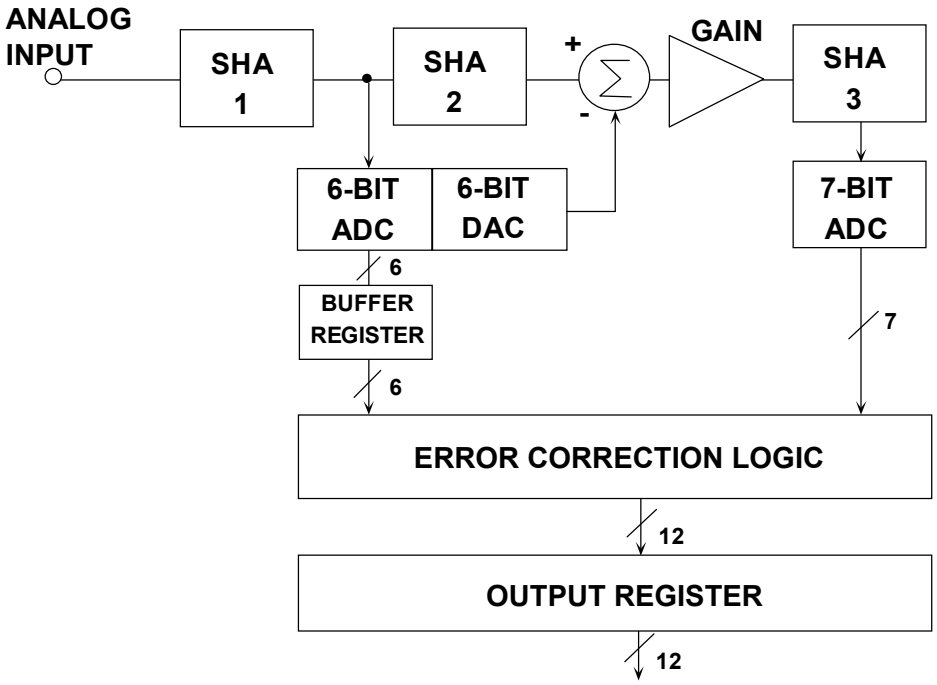


Figure 3.25

The second SHA delays the held output of the first SHA while the first-stage conversion occurs, thereby maximizing throughput. The third SHA serves to *deglitch* the residue output signal, thereby allowing a full conversion cycle for the 7-bit ADC to make its decision (the 6 and 7-bit ADCs in the AD6640 are bit-serial *MagAmp* ADCs which require more settling time than a flash converter).

This multi-stage conversion technique is sometimes referred to as "pipelining." Additional shift registers in series with the digital outputs of the first-stage ADC ensure that its output is ultimately time-aligned with the last 7 bits from the second ADC when their outputs are combined in the error correction logic. A pipelined ADC therefore has a specified number of clock cycles of *latency*, or *pipeline delay* associated with the output data. The leading edge of the sampling clock (for sample N) is used to clock the output register, but the data which appears as a result of that clock edge corresponds to sample N – L, where L is the number of clock cycles of latency. In the case of the AD6640, there are two clock cycles of latency.

The error correction scheme described above is designed to correct for errors made in the first conversion. Internal ADC gain, offset, and linearity errors are corrected as long as the residue signal falls within the range of the second-stage ADC. These errors will not affect the linearity of the overall ADC transfer characteristic. Errors made in the final conversion, however, do translate directly as errors in the overall transfer function. Also, linearity errors or gain errors either in the DAC or the residue amplifier will not be corrected and will show up as nonlinearities or non-monotonic behavior in the overall ADC transfer function.

So far, we have considered only two-stage subranging ADCs, as these are easiest to analyze. There is no reason to stop at two stages, however. Three-pass and four-pass subranging pipelined ADCs are quite common, and can be made in many different ways, usually with digital error correction.

A simplified block diagram of the AD9220 12-bit, 10MSPS single-supply, 250mW CMOS ADC is shown in Figure 3.26. The AD9221 (1.25MSPS, 60mW) and the AD9223 (3MSPS, 100mW) ADCs use the identical architecture but operate at lower power and lower sampling rates. This is a four-stage pipelined architecture with an additional bit in the second, third, and fourth stage for error correction. Because of the pipelined architecture, these ADCs have a 3 clock-cycle latency (see Figure 3.27).

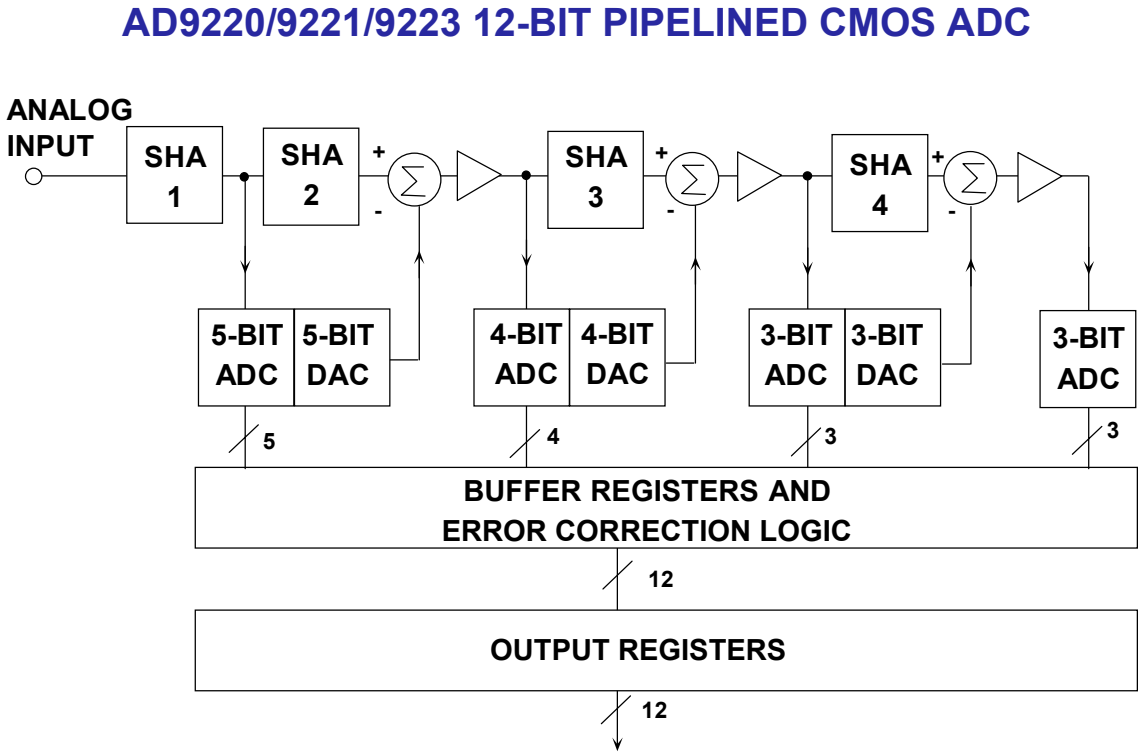


Figure 3.26

LATENCY (PIPELINE DELAY) OF AD9220/9221/9223 ADC

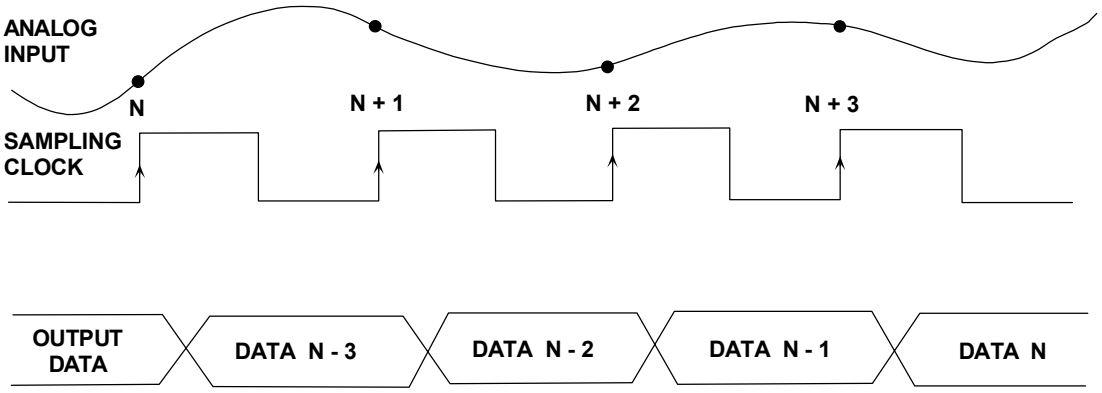


Figure 3.27

BIT-PER-STAGE (SERIAL, OR RIPPLE) ADCs

Various architectures exist for performing A/D conversion using one stage per bit. In fact, a multistage subranging ADC with one bit per stage and no error correction is one form. Figure 3.28 shows the overall concept. The SHA holds the input signal constant during the conversion cycle. There are N stages, each of which have a bit output and a residue output. The residue output of one stage is the input to the next. The last bit is detected with a single comparator as shown.

BIT-PER-STAGE, SERIAL, OR RIPPLE ADC

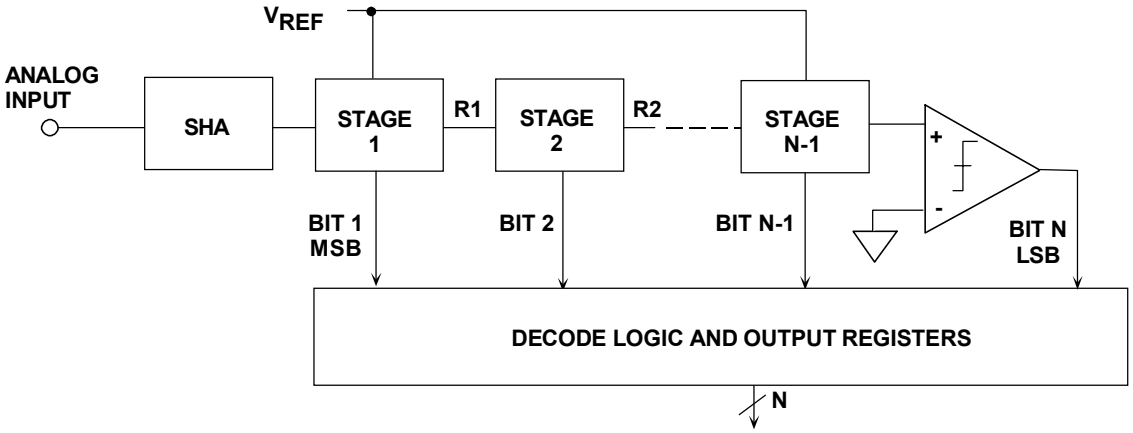


Figure 3.28

The basic stage for performing a single binary bit conversion is shown in Figure 3.29. It consists of a gain-of-two amplifier, a comparator, and a 1-bit DAC. Assume that this is the first stage of the ADC. The MSB is simply the polarity of the input, and that is detected with the comparator which also controls the 1-bit DAC. The 1-bit DAC output is summed with the output of the gain-of-two amplifier. The resulting residue output is then applied to the next stage. In order to better understand how the circuit works, the diagram shows the residue output for the case of a linear ramp input voltage which traverses the entire ADC range, $-V_R$ to $+V_R$. Notice that the polarity of the residue output determines the binary bit output of the next stage.

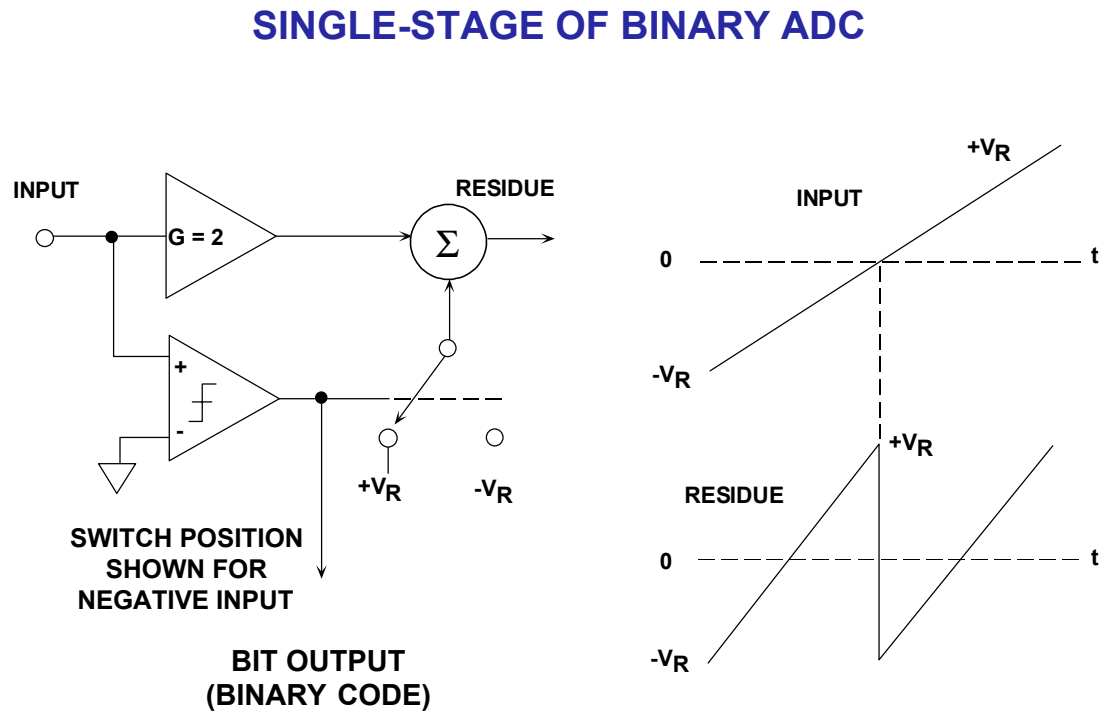


Figure 3.29

A simplified 3-bit serial-binary ADC is shown in Figure 3.30, and the residue outputs are shown in Figure 3.31. Again, the case is shown for a linear ramp input voltage whose range is between $-V_R$ and $+V_R$. Each residue output signal has discontinuities which correspond to the point where the comparator changes state and causes the DAC to switch. The fundamental problem with this architecture is the discontinuity in the residue output waveforms. Adequate settling time must be allowed for these transients to propagate through all the stages and settle at the final comparator input. The prospects of making this architecture operate at high speed are therefore dismal.

3-BIT SERIAL ADC WITH BINARY OUTPUT

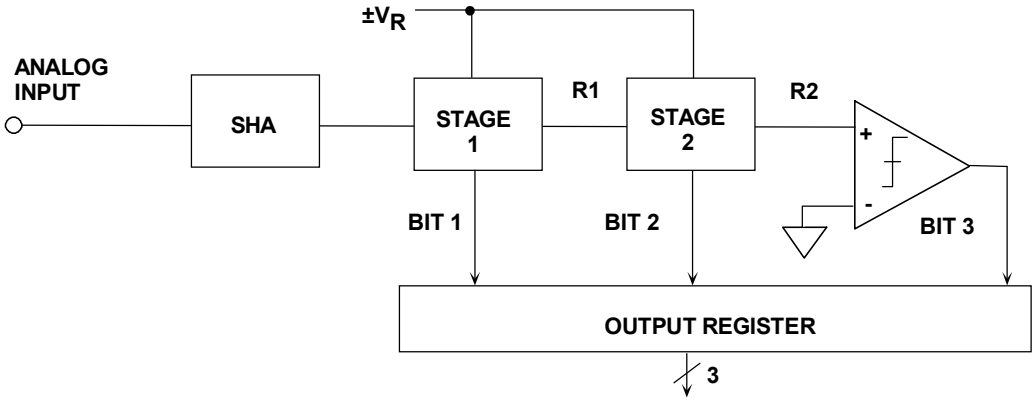


Figure 3.30

INPUT AND RESIDUE WAVEFORMS OF 3-BIT BINARY RIPPLE ADC

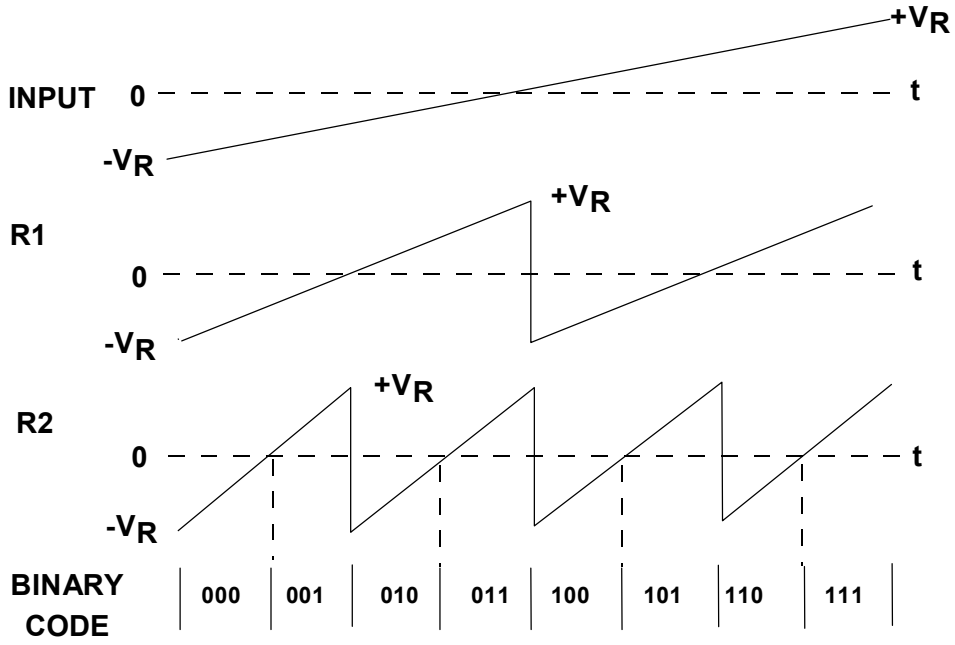


Figure 3.31

A much better bit-per-stage architecture was developed by F.D. Waldhauer (Reference 21) based on absolute value amplifiers (magnitude amplifiers, or simply *MagAmps*™). This scheme has often been referred to as *serial-Gray* (since the output coding is in Gray code), or *folding* converter (References 22, 23, 24). The basic stage is shown functionally in Figure 3.32 along with its transfer function. The input to the stage is assumed to be a linear ramp voltage whose range is between

$-V_R$ and $+V_R$. The comparator detects the polarity of the input signal and provides the Gray bit output for the stage. It also determines whether the overall stage gain is +2 or –2. The reference voltage V_R is summed with the switch output to generate the residue signal which is applied to the next stage. The polarity of the residue signal determines the Gray bit for the next stage. The transfer function for the folding stage is also shown in Figure 3.32.

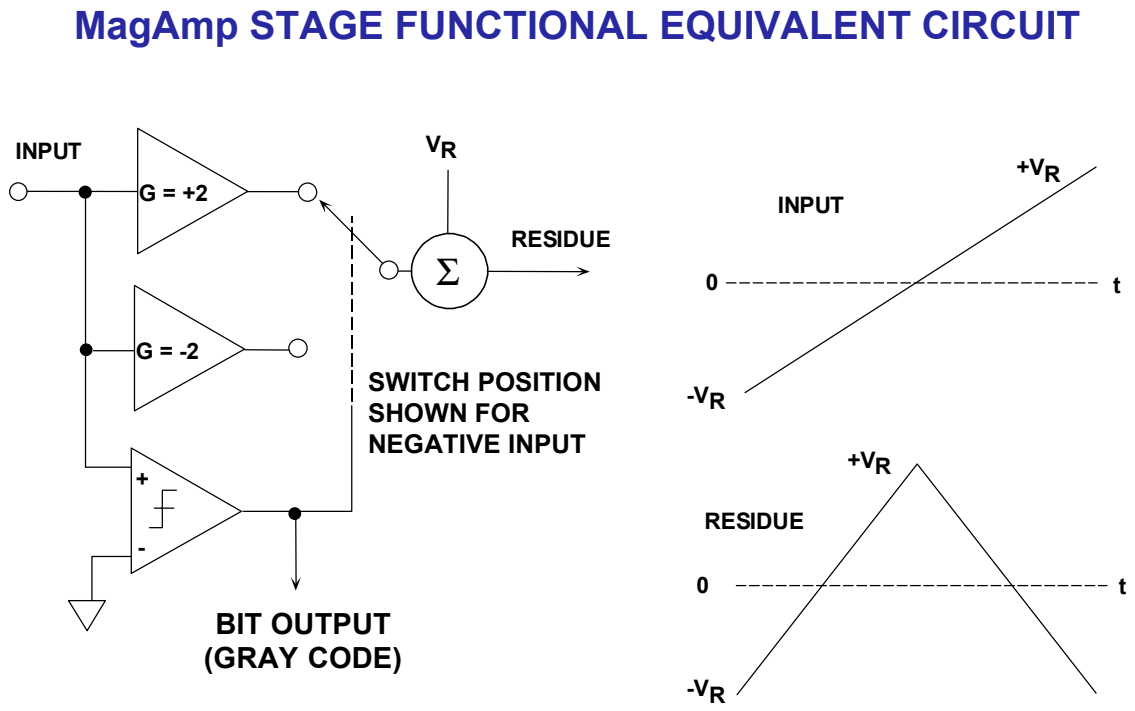


Figure 3.32

A 3-bit MagAmp folding ADC is shown in Figure 3.33, and the corresponding residue waveforms in Figure 3.34. As in the case of the binary ripple ADC, the polarity of the residue output signal of a stage determines the value of the Gray bit for the next stage. The polarity of the input to the first stage determines the Gray MSB; the polarity of R1 output determines the Gray bit-2; and the polarity of R2 output determines the Gray bit-3. Notice that unlike the binary ripple ADC, there is no abrupt transition in any of the folding stage residue output waveforms. This makes operation at high speeds quite feasible.

The key to operating this architecture at high speeds is the folding stage. Early designs (see References 22, 23, 24) used discrete op amps with diodes inside the feedback loop to generate the folding transfer function. Modern IC circuit designs implement the transfer function using current-steering open-loop gain techniques which can be made to operate much faster. Fully differential stages (including the SHA) also provide speed, lower distortion, and yield 8-bit accurate folding stages with no requirement for thin film resistor laser trimming (see References 25, 26, 27).

3-BIT MagAmp™ (FOLDING) ADC BLOCK DIAGRAM

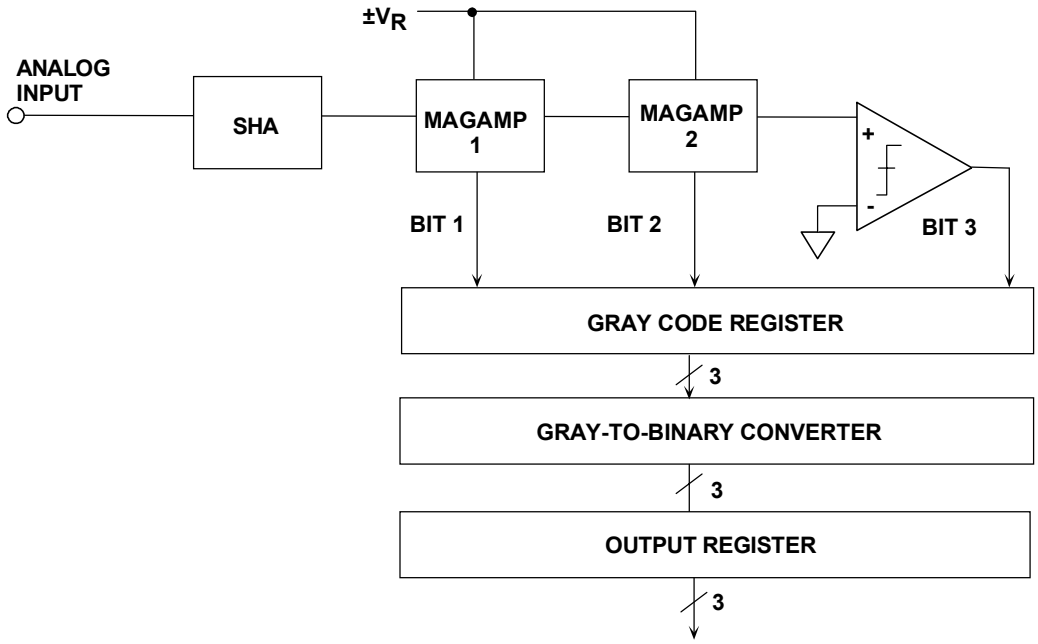


Figure 3.33

INPUT AND RESIDUE WAVEFORMS FOR 3-BIT MagAmp ADC

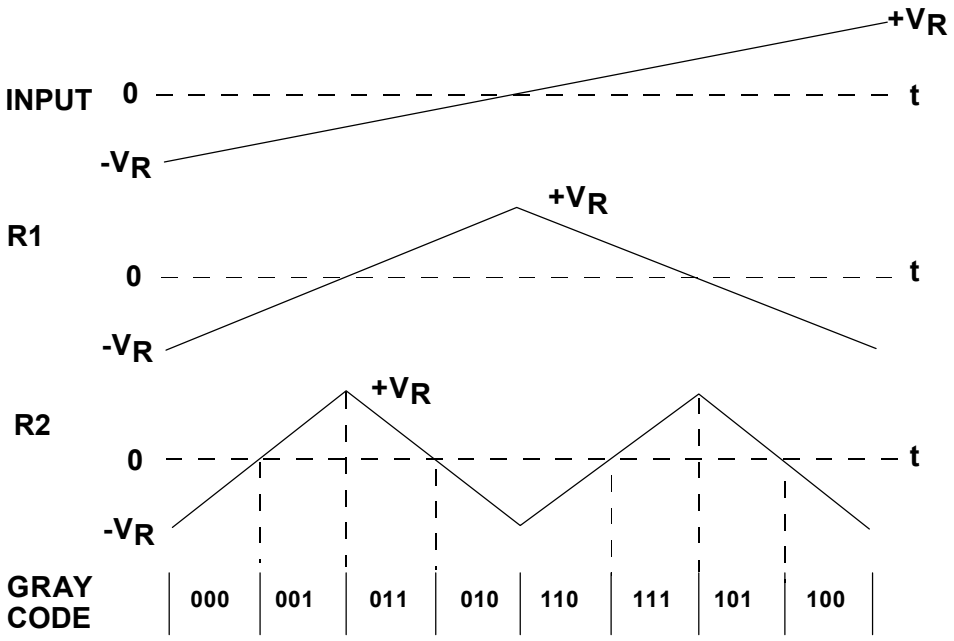


Figure 3.34

The MagAmp architecture can be extended to sampling rates previously dominated by flash converters. The AD9288-100 8-bit, 100MSPS dual ADC is shown in Figure 3.35. The first five bits (Gray code) are derived from five differential MagAmp stages. The differential residue output of the fifth MagAmp stage drives a 3-bit flash converter, rather than a single comparator. The Gray-code output of the five MagAmps and the binary-code output of the 3-bit flash are latched, all converted into binary, and latched again in the output data register.

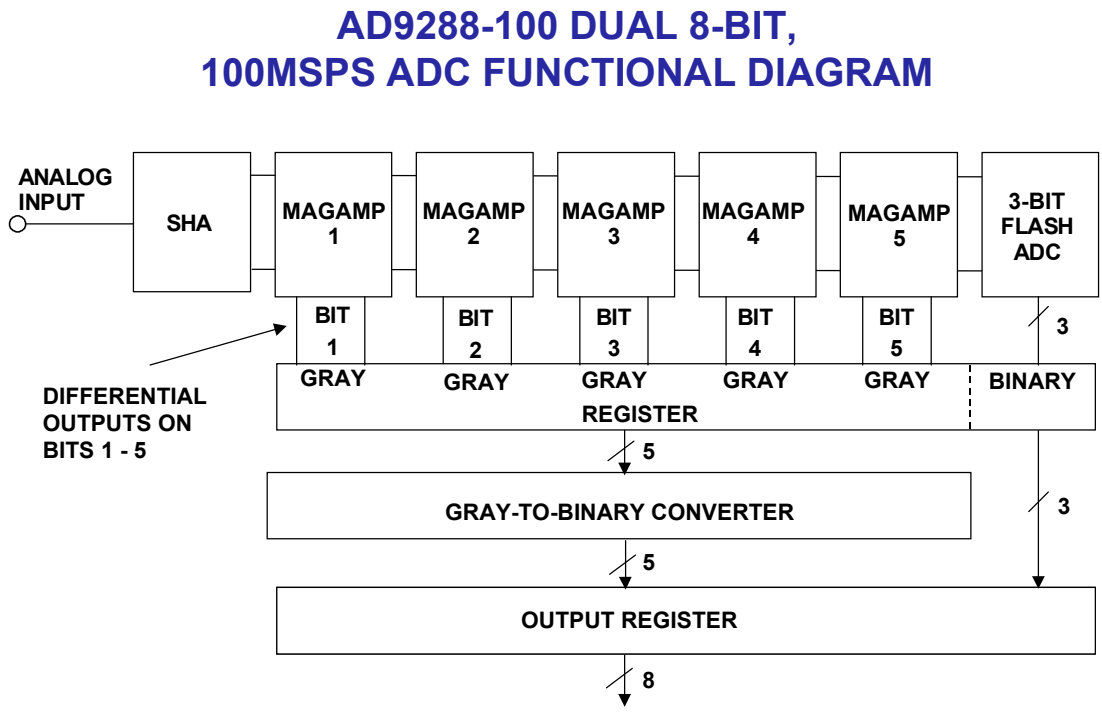


Figure 3.35

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